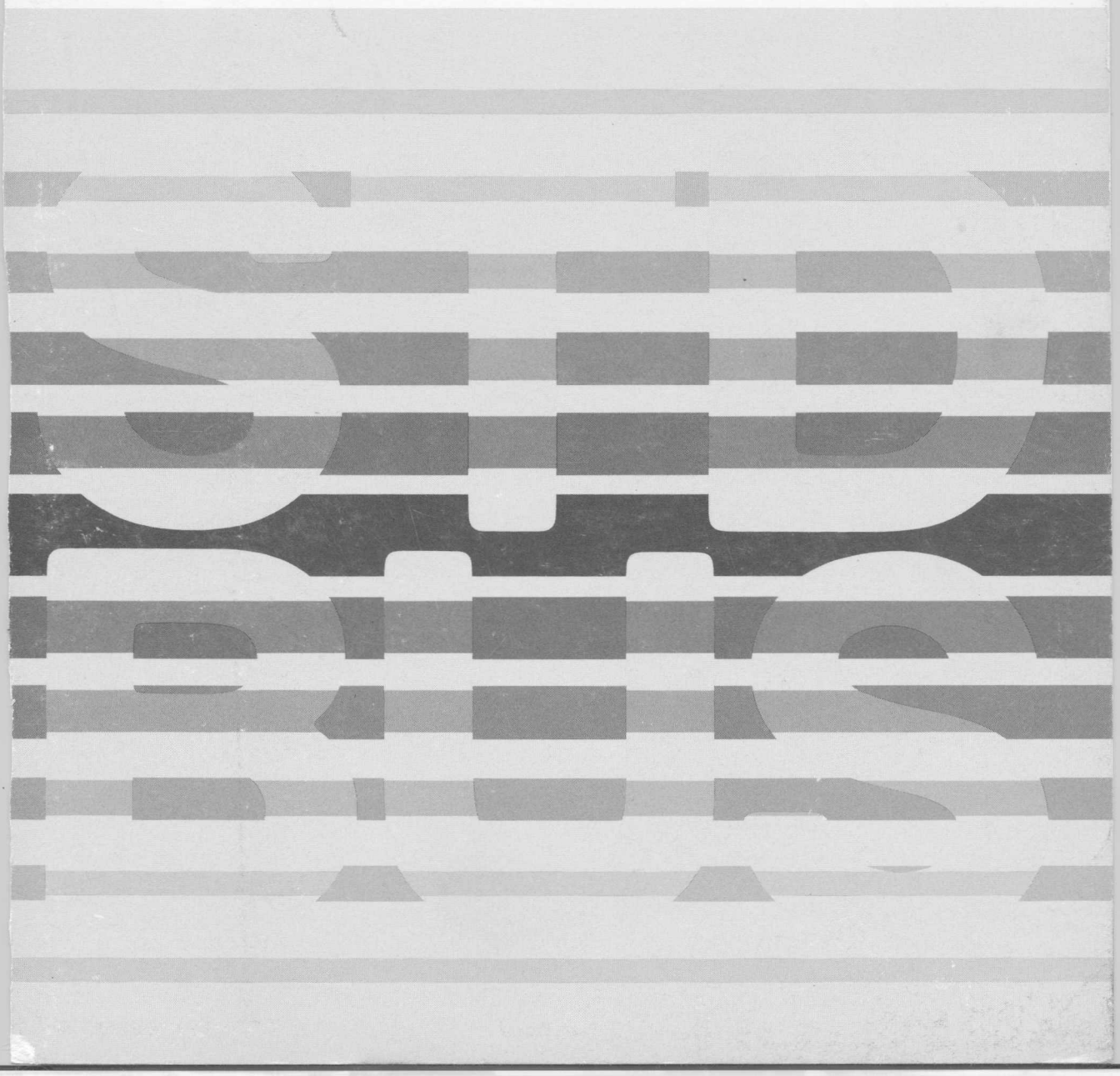
PRO-LOG
CORPORATION

SERIES 7000
STD BUS

TECHNICAL MANUAL
AND PRODUCT CATALOG

July 1981



Series 7000 STD BUS
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FOREWORD

This manual is aimed primarily at the professional design engineer who contemplates using the STD BUS in his company's products. It defines the standards that constitute the STD BUS. It also defines the parameters that are common to the Series 7000 cards. The Series 7000 Data Sheets are included to illustrate the compatibility of the Series 7000 cards and to provide design guidelines and application information.

The STD BUS is a concept conceived by Pro-Log Corporation and developed jointly with MOSTEK as a simple bus structure for 8-bit microprocessors. It is a 56-pin bus, logically organized and easily learned. The number of pins and their use is a well-thought-out compromise between the simplest possible bus and an infinitely flexible bus. The bus is kept simple to facilitate design, production, and maintenance. It is made sufficiently flexible to work with all industry standard 8-bit microprocessors and to be used in both dedicated control and data processing applications.

The company that uses STD BUS hardware in its products generally wants to control the design, production, and maintenance of such products with his existing personnel. Pro-Log's Series 7000 hardware helps him attain this goal, because it is modular, standardized, uses only second-sourced industry standard parts, is thoroughly documented, and has a manufacturing rights option that allows Pro-Log customers to produce the STD 7000 products themselves, if they wish.

Pro-Log also teaches courses on how to design with, and use microprocessors and the STD BUS products: instruments such as PROM programmers and system analyzers with which to manufacture and service STD BUS products.

THE STD BUS PROVIDES

- Standard 8-bit microprocessor Bus pinout
- Standard 56-pin connector
- Standard 4.5 x 6.5 in. (114.30 x 165.10 mm) card size
- Standard ½ in. (12.7 mm) card spacing

THE STD BUS OFFERS

- Multiple sources
- Unrestricted use, not trademarked, copyrighted or patented
- Function modularity
- Card slot independence
- Separate digital and analog power busses

THE SERIES 7000 CARDS ADD

- Motherboard interconnect
- High functional density
- Low power consumption
- Industry standard components
- Second-sourced components
- Completely tested cards
- Power-on burn-in
- RETMA rack mounting compatible card cages
- Choice of microprocessor

Contents

SECTION 1
STD BUS Specification

Introduction

The STD BUS standardizes the physical and electrical aspects of modular 8-bit microprocessor card systems. It provides a dedicated and orderly interconnection scheme (Fig. 1-1). The standardized pinout and 56-pin connector lend themselves to a bussed motherboard that permits any card to work in any slot.

The STD BUS is dedicated to internal communications. All other interconnections are made via suitable connectors at the I/O interface card edge. The concept gives an orderly signal flow across the cards. Peripheral and I/O devices can be connected to the system, according to their own unique connector and cabling requirements.

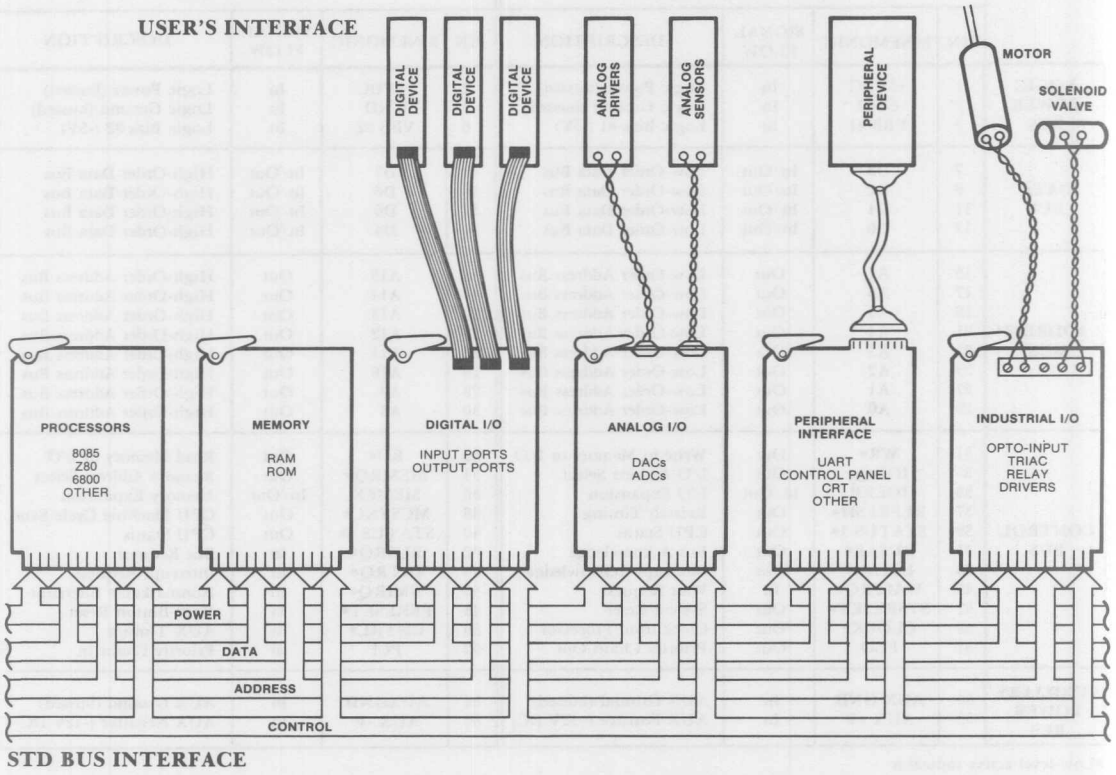


Figure 1-1. STD BUS Implementation.

Organization and Functional Specifications (with pin definitions)

The STD BUS pinout is organized into four functional groups:

- Dual Power Busses: Pins 1-6 and 53-56
- Data Bus: Pins 7-14
- Address Bus: Pins 15-30
- Control Bus: Pins 31-52

The organization and pinouts are shown in Table 1-1. This table lists the mnemonic function and signal flow direction (referenced to the processor card in control of the BUS) for each pin of the STD BUS. The STD BUS is further defined as requiring a 56-pin (dual 28) card edge connector, with 0.125-in. pin centers. Connectors are on a spacing interval of 0.5-in. centers minimum, and they accept the standard 4.5 x 6.5 x 0.062-in. card.

Table 1-1. STD BUS Pinouts with Signal Flow Referenced to the Processor Card.

	COMPONENT SIDE				CIRCUIT SIDE			
	PIN	MNEMONIC	SIGNAL FLOW	DESCRIPTION	PIN	MNEMONIC	SIGNAL FLOW	DESCRIPTION
LOGIC POWER BUS	1	+5VDC	In	Logic Power (bussed)	2	+5VDC	In	Logic Power (bussed)
	3	GND	In	Logic Ground (bussed)	4	GND	In	Logic Ground (bussed)
	5	VBB #1	In	Logic Bias #1 (-5V)	6	VBB #2	In	Logic Bias #2 (-5V)
DATA BUS	7	D3	In/Out	Low-Order Data Bus	8	D7	In/Out	High-Order Data Bus
	9	D2	In/Out	Low-Order Data Bus	10	D6	In/Out	High-Order Data Bus
	11	D1	In/Out	Low-Order Data Bus	12	D5	In/Out	High-Order Data Bus
	13	D0	In/Out	Low-Order Data Bus	14	D4	In/Out	High-Order Data Bus
ADDRESS BUS	15	A7	Out	Low-Order Address Bus	16	A15	Out	High-Order Address Bus
	17	A6	Out	Low-Order Address Bus	18	A14	Out	High-Order Address Bus
	19	A5	Out	Low-Order Address Bus	20	A13	Out	High-Order Address Bus
	21	A4	Out	Low-Order Address Bus	22	A12	Out	High-Order Address Bus
	23	A3	Out	Low-Order Address Bus	24	A11	Out	High-Order Address Bus
	25	A2	Out	Low-Order Address Bus	26	A10	Out	High-Order Address Bus
	27	A1	Out	Low-Order Address Bus	28	A9	Out	High-Order Address Bus
	29	A0	Out	Low-Order Address Bus	30	A8	Out	High-Order Address Bus
CONTROL BUS	31	WR*	Out	Write to Memory or I/O	32	RD*	Out	Read Memory or I/O
	33	IORQ*	Out	I/O Address Select	34	MEMRQ*	Out	Memory Address Select
	35	IOEXP	In/Out	I/O Expansion	36	MEMEX	In/Out	Memory Expansion
	37	REFRESH*	Out	Refresh Timing	38	MCSYNC*	Out	CPU Machine Cycle Sync.
	39	STATUS 1*	Out	CPU Status	40	STATUS 0*	Out	CPU Status
	41	BUSAK*	Out	Bus Acknowledge	42	BUSRQ*	In	Bus Request
	43	INTAK*	Out	Interrupt Acknowledge	44	INTRQ*	In	Interrupt Request
	45	WAITRQ*	In	Wait Request	46	NMIRQ*	In	Nonmaskable Interrupt
	47	SYSRESET*	Out	System Reset	48	PBRESET*	In	Push-Button Reset
	49	CLOCK*	Out	Clock from Processor	50	CNTRL*	In	AUX Timing
	51	PCO	Out	Priority Chain Out	52	PCI	In	Priority Chain In
AUXILIARY POWER BUS	53	AUX GND	In	AUX Ground (bussed)	54	AUXGND	In	AUX Ground (bussed)
	55	AUX +V	In	AUX Positive (+12V DC)	56	AUX -V	In	AUX Negative (-12V DC)

*Low-level active indicator

Dual Power Busses (Pins 1-6 and 53-56). The dual power busses accommodate logic and analog power distribution. As many as five separate power supplies can be used with two separate ground returns as shown.

PIN	DESCRIPTION	COMMENTS
1 & 2	Logic Power	Logic Power Source (+15V DC
3 & 4	Logic Ground	Logic Power Return Bus
5	Logic Bias Voltage	Low-current Logic Supply #1 (-5V)
6	Logic Bias Voltage	Low-current Logic Supply #2 (-5V)
53 & 54	Auxiliary Ground	Auxiliary Power Return Bus
55	Auxiliary Positive	Positive DC Supply (+12V)
56	Auxiliary Negative	Negative DC Supply (-12V)

Data Bus (Pins 7-14). The data bus is an 8-bit, bidirectional, 3-state bus. (Bidirectional means signals may flow either into or out of any card on the bus.) Direction of data is normally controlled by the processor card via the control bus. The data direction is normally affected by such signals as read (RD*), write (WR*), and interrupt acknowledge (INTAK*.)

The data bus uses high-level active logic. All cards are required to release the bus to a high-impedance state when not in use. The processor card releases the data bus in response to bus request (BUSRQ*) input from an alternate system controller, as in DMA transfers.

Address Bus (Pins 15-30). The address bus is a 16-bit, 3-state, high-level active bus. Normally, the address originates at the processor card. The card releases the address bus in response to a BUSRQ* input from an alternate controller.

The address bus provides 16 address lines for decoding by either memory or I/O. Memory request (MEMRQ*) and I/O request (IORQ*) control lines distinguish between the two operations. The particular microprocessor that you use determines the number of address lines and how they are applied.

Example:

PROCESSOR	NO. OF MEM ADR. LINES	ADDRESS LINES DURING REFRESH	NO. OF I/O ADDRESS LINES	
			I/O MAPPED I/O	MEMORY MAPPED I/O
8080	16	—	Lower 8	16
8085	16	—	Lower 8	16
Z80	16	Lower 7	Lower 8	16
6800	16	—	—	16
6809	16	—	—	16
6502	16	—	—	16
NSC800	16	Lower 7	Lower 8	16

Control Bus (Pins 31-52). The control bus determines the flexibility of the STD BUS. Signal lines are grouped into five separate areas: memory and I/O control, peripheral timing, clock and reset, interrupt and bus control, and serial priority chain.

Memory and I/O Control lines provide the signals for fundamental memory and I/O operations. Simple applications may only require the following six control signals:

- WR*—Write to memory or I/O (3-state, active-low), pin 31.

  This signal indicates that the BUS holds valid data to be written in the addressed memory or output device. WR* is the clock pulse, which writes data to memory or output port latches. The signal originates from the processor, which also provides the output data on the BUS.

- RD*—Read from memory or I/O (3-state, active-low), pin 32.

  This signal indicates that the processor or other bus-controlling device needs to read data from memory or from an I/O device. The selected I/O device or memory utilizes this signal to gate data onto the BUS. RD* originates from the processor, which accepts the data from the BUS.

- IORQ*—I/O address select (3-state, active-low), pin 33.

  This signal indicates that the address lines hold a valid I/O address for an I/O read or write. It is used on the I/O cards and is gated with either RD* or WR* to designate I/O operations.

- MEMRQ*—Memory address select (3-state, active-low), pin 34.

  This signal indicates that the address bus holds a valid address for memory read or memory write operations. It is used on memory cards and is gated with either RD* or WR* to designate memory operations.

- IOEXP—I/O expansion (high expand, low enable), pin 35.

  This signal expands or enables I/O port addressing. An active-low enables primary I/O operations. An example of its use is to allow common address decoding in memory-mapped I/O operations. Simple systems can generally strap this signal to ground.

- MEMEX—Memory expansion (high expand, low enable), pin 36.

  This signal expands or enables memory addressing. An active-low enables the primary system memory. MEMEX allows memory overlay such as that found in bootstrap operations. A control card may switch out the primary system memory to make use of an alternate memory. Simple systems can generally strap this signal to ground.

Peripheral Timing Control lines provide control signals that enable the use of the STD BUS with microprocessors that service their own peripheral devices. The STD BUS is intended to service any 8-bit microprocessor. Most peripheral devices work only with the microprocessor they are designed for. Four control lines of the STD BUS are designated for peripheral timing. They are defined specifically for each type of microprocessor, so that it can best serve its own peripheral devices. In this way, the STD BUS is not limited to only one processor.

- REFRESH*—(3-state, active-low), pin 37.

  This signal refreshes dynamic memory. It may be generated on the processor card or on a separate control card. The nature and timing of the signal may be a function of the memory device or of the microprocessor. In systems without refresh, this signal can be any specialized memory control signal. Simple systems with static memory may disregard REFRESH*.

- MCSYNC*—Machine cycle sync (3-state, active-low), pin 38.

  This signal occurs once during each machine cycle of the processor. (Machine cycle is defined as the sequence that involves addressing, data transfer, and execution.) MCSYNC* defines the beginning of the machine cycle. The exact nature and timing of this signal are processor-dependent. MCSYNC* keeps specialized peripheral devices synchronized with the processor's operation. It can also be used for controlling a bus analyzer, which can analyze bus operations cycle-by-cycle.

- STATUS 1*—Status control line 1 (3-state, active-low), pin 39.

  This signal provides secondary timing for peripheral devices. When available, STATUS 1* is considered as a signal for identifying instruction fetch.

- STATUS 0*—Status control line 0 (3-state, active-low), pin 40.

  This signal provides additional timing for peripheral devices.

Table 1-2 defines the peripheral timing-control lines for various 8-bit microprocessors. The designated pins are also being defined for other microprocessors.

Table 1-2. Peripheral Timing-Control Lines for Various 8-Bit Microprocessors.

	REFRESH*	MCSYNC*	STATUS 1*	STATUS 0*
	PIN 37	PIN 38	PIN 39	PIN 40
8080	—	SYNC*	M1*	—
8085	—	ALE*	S1*	SO*
NSC800	REFRESH*	ALE*	S1*	SO*
8088	—	ALE*	DT/R*	SSO*
Z80	REFRESH*	(RD*+WR*+INTAK*)	M1*	—
6800	—	Ø2*	VMA*	R/W*
6809	—	EOUT* (Ø2*)	—	R/W*
6809E	—	EOUT* (Ø2*)	LIC*	R/W*
6502	—	Ø2*	SYNC*	R/W*

* Low-level active
— Not used
R/W* Read high, write low
DT/R* Data transmit high, receive low

Interrupt and bus control lines allow the implementation of such bus control schemes as direct memory access, multiprocessing, single stepping, slow memory, power-fail-restart, and a variety of interrupt methods. The STD BUS includes provision for a serial priority chain. Parallel priority schemes can also be implemented.

- BUSAK*—Bus acknowledge (active-low), pin 41.

  This signal indicates that the bus is available for use by a requesting controller. The controlling processor responds to a BUSRQ* by releasing the BUS and giving an acknowledge signal on the BUSAK* line. BUSAK* occurs at the completion of the current machine cycle.

- BUSRQ*—Bus request (active-low, open collector), pin 42.

  This signal causes the controlling processor to suspend operations on the STD BUS by releasing all 3-state STD BUS lines for use by another processor. The STD BUS is released when the current machine cycle has been completed. BUSRQ* is used in applications requiring direct memory access (DMA). In complex systems, it can be an input, or an output, or it can be bidirectional, depending on the supporting hardware.

- INTAK*—Interrupt acknowledge (active-low), pin 43.

  This signal tells the interrupting device that the processor card is ready to respond to the interrupt. For vectored interrupts, the interrupting device places the vector address on the data bus during INTAK*. This signal can be combined with a priority signal, if multiple controllers need bus access. INTAK* is not used in nonvectored interrupt schemes.

- INTRQ*—Interrupt request (active-low, open collector), pin 44.

  This processor-card input signal conditionally interrupts the program. It is masked and ignored by the processor, unless deliberately enabled by a program instruction. If the processor accepts the interrupt, it usually acknowledges by dropping INTAK* (pin 43). Other actions depend on the specific type of processor, the interrupt-related program instructions, and the hardware support of the interrupt mechanism.

- WAITRQ*—Wait request (active-low, open collector), pin 45.

  This input signal to the processor suspends operations as long as it remains low. Normally, the processor holds in a state that maintains a valid address on the address bus. WAITRQ* can be used to insert wait states in the processor cycle. Examples of its use include slow-memory operations and single stepping.

- NMIRQ*—Nonmaskable interrupt (active-low, open collector), pin 46.

  This signal is a processor-card interrupt input of the highest priority. It should be used for critical processor signalling, e.g., power-fail indications.

Clock and reset lines provide the STD BUS with basic clock timing and reset capability.

- SYSRESET*—System reset (active-low), pin 47.

  This signal is an output from the system reset circuit, which is triggered by power-on detection, or by the push-button reset. The system reset bus line should be applied to all bus cards that have latch circuits requiring initialization.

- PBRESET*—Push-button reset (active-low), pin 48.

  This signal is an input line to the system reset circuit.

- CLOCK*—Clock from processor, pin 49.

  This signal is a buffered, processor clock signal, for use in system synchronization or as a general clock source.

- CNTRL*—Control, pin 50.

  This signal is an auxiliary circuit for special clock timing. It may be a multiple of the processor clock signal, a real-time clock signal, or an external input to the processor.

Serial priority chain lines are provided for interrupt or bus control. Two bus pins are allocated to the chain, which requires logic on the card to implement the priority function. Cards not needing the chain must jumper PCI to PCO on the card, if they are to be used in a serial priority scheme.

- PCO—Priority chain out, pin 51.

  This signal is sent to the PCI input of the next lower card in priority. A card that needs priority should hold PCO low.

- PCI—Priority chain in, pin 52.

  This signal is provided directly from the PCO of the next higher card in priority. A high level on PCI gives priority to the card sensing the PCI input.

Electrical Specifications

Absolute Maximum Ratings. The maximum ratings for the STD BUS card edge connector pins, which are listed below, are not recommended operating conditions. Above these values, damage to card components is possible. The specific voltage at which damage occurs is component-dependent.

PARAMETER	LIMIT	REFERENCE
Positive voltage applied to logic input or disabled 3-state output	+5.5V	GND pins 3, 4
Negative DC voltage applied to a logic input or disabled 3-state output	-0.4V	

Note: Unless otherwise specified, the removal of circuit cards that are compatible with the STD BUS, or the removal of their component parts from sockets, is not recommended while operating voltages are applied.

Power Bus Voltage Tolerances. STD BUS cards normally require +5V for logic operations. Other operating voltages may be needed, according to individual card function and device types. The table below shows the STD BUS power busses and voltage values. Note that these voltage values are specified at the card pins, not at the backplane traces.

CARD PIN	SUPPLY VOLTAGE	TOLERANCE	REFERENCE
1, 2	VCC (+5V)	±0.25V	GND pins 3, 4
5	VBB #1 (-5V)	±0.25V	GND pins 3, 4
6	VBB #2 (-5V)	±0.25V	GND pins 3, 4
55	AUX +V (+12V)	±0.5V	AUX GND pins 53, 54
56	AUX -V (-12V)	±0.5V	AUX GND pins 53, 54

Logic Signal Characteristics. The STD BUS is designed for compatibility with industry-standard TTL logic. The following specifications apply over the specified temperature range for the STD BUS.

STD BUS CARD PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
VOH (high-state output voltage)	VCC=MIN	IOH=-15 mA	2.4	—	V
VOL (low-state output voltage)	VCC=MIN	IOL=24mA	—	0.5	V
VIH (high-state input voltage)			2.0	—	V
VIL (low-state input voltage)			—	0.8	V
tR, tF (rise time, fall time)			4	100	NS

Mechanical Specifications

The circuit card size and outline of the STD BUS are defined in Table 1-3 and Figures 1-2 and 1-3. The dimensions exclude the card ejector and I/O interface connections.

Table 1-3. STD BUS Card Dimensions.

STD CARD DIMENSIONS	INCHES		MILLIMETERS	
	NOMINAL	TOLERANCE	NOMINAL	TOLERANCE
Card Length	6.500	±0.025	165.10	±0.64
Card Height	4.500	+0.005, -0.025	114.30	+0.13, -0.64
Plated Board Thickness	0.062	±0.003	1.58	±0.08
Card Spacing	0.500	MIN	12.70	MIN

Minimum card spacing requires a consideration for component height, lead protrusion, and card clearance, in addition to the board thickness. Table 1-4 lists recommended dimensions for these parameters; however, trade-offs can be made between component height and lead protrusion. Cards not meeting these requirements may need multiple card slot positions.

Table 1-4. STD BUS Profile Dimensions for Minimum Spacing.

RECOMMENDED DIMENSIONS FOR MINIMUM CARD SPACING	INCHES		MILLIMETERS	
	MAXIMUM	MINIMUM	MAXIMUM	MINIMUM
Component Height	0.375	—	9.52	—
Component Lead Protrusion ⚠	0.040	—	1.02	—
Adjacent Card Clearance	—	0.010	—	0.25

⚠ The card ejector occupies the top 1.4-in. (35.6 mm) of the card and protrudes 0.1-in. (2.54 mm) on each side of the card.

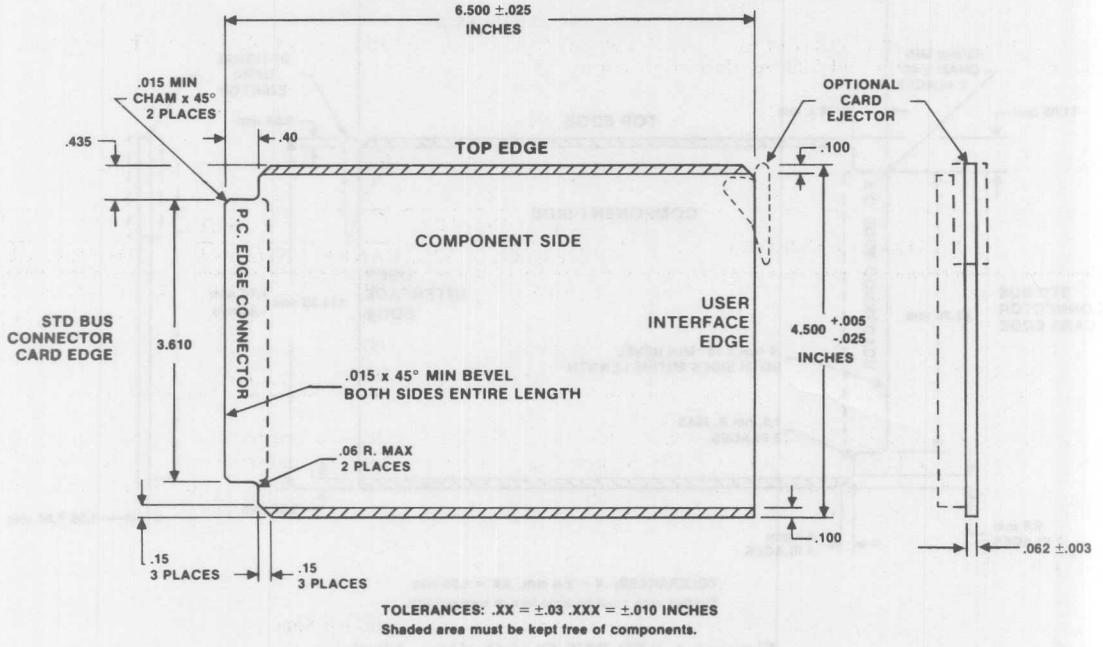


Figure 1-2. STD BUS Card Outline.

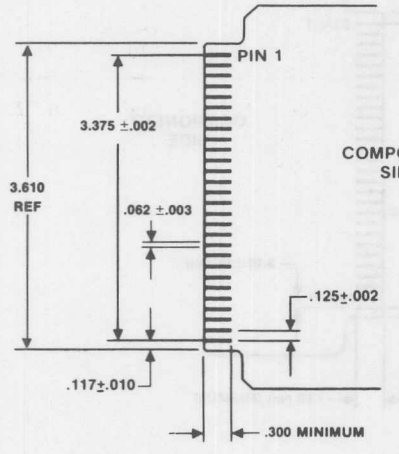


Figure 1-3. STD BUS Edge Card Finger Design.

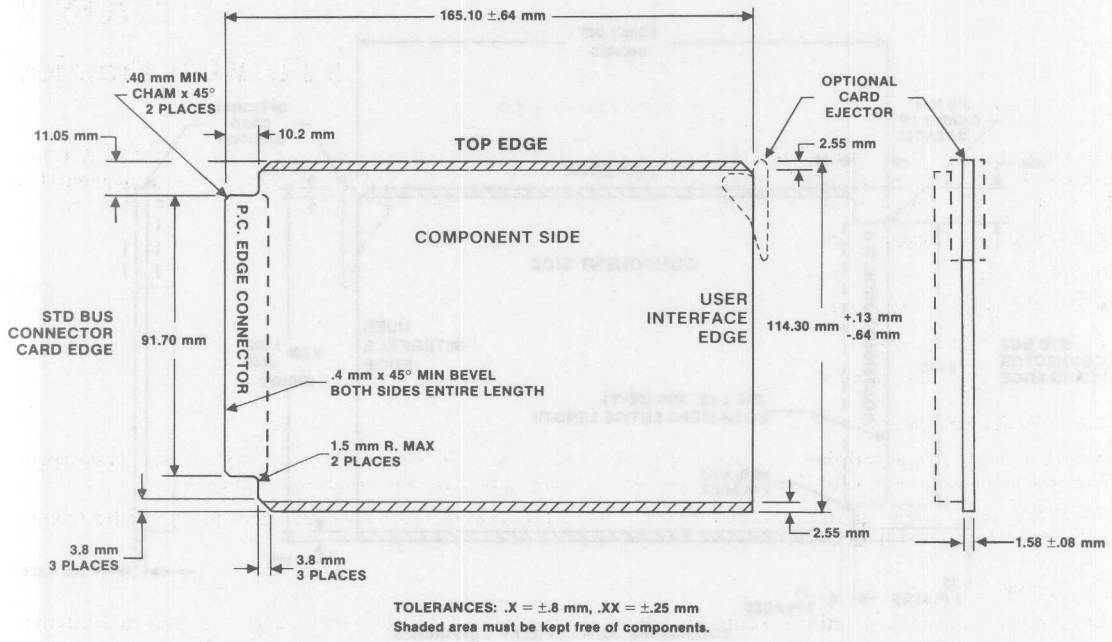


Figure 1-4. STD BUS Card Outline - Metric.

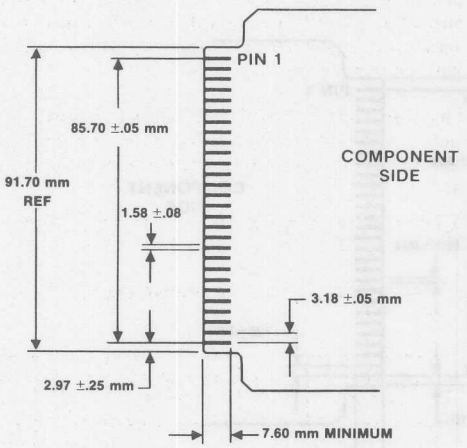


Figure 1-5. STD BUS Edge Card Finger Design - Metric.

SECTION 2
STD BUS Practice

The industry-based STD Manufacturers Group meets regularly to review concerns regarding the STD BUS. It has resolved the following recommended practice for the design of STD BUS cards. The STD Practice is supplemental to the STD Specification and is to be applied at the discretion of the user. The current STD Practice relates to:

- Compatibility designation
- Bus timing
- Parallel priority interrupt
- Card keying for polarity
- Open collector bus signals

Compatibility Designation

STD BUS cards that use peripheral chips usually depend on specific timing signals from the processor. This dependency prevents peripheral cards from being used interchangeably with cards from other families.

The STD Practice for designating compatibility is to label cards that are processor-timing-dependent, with reference to the CPU device: STD-Z80, STD-8085, STD-6800, etc.

Bus Timing

Card designers require bus timing definitions to insure compatibility. The recommended STD Practice for cards that source the bus control signals is for each card to specify the waveforms and timing information. Bus timing is further defined in the STD-Z80 and STD-8085 specifications.

Parallel Priority Interrupt

The STD BUS provides signal lines for interrupt requests and bus requests. In systems with only a single interrupting device or a single alternate controller, these lines are sufficient to allow direct implementation. But in systems with multiple interrupting devices or multiple bus controllers, a priority scheme is necessary. The STD BUS is designed to handle either serial priority or parallel priority schemes.

Serial Priority. The STD BUS includes a priority-chain bus signal for serial priority schemes. Serial priority, using PCI and PCO signals, requires that each peripheral needing priority must have logic on the card to service the request, as shown in Figure 2-1. This scheme is practical with peripheral devices designed to service a serial priority chain such as the Z80 family of devices.

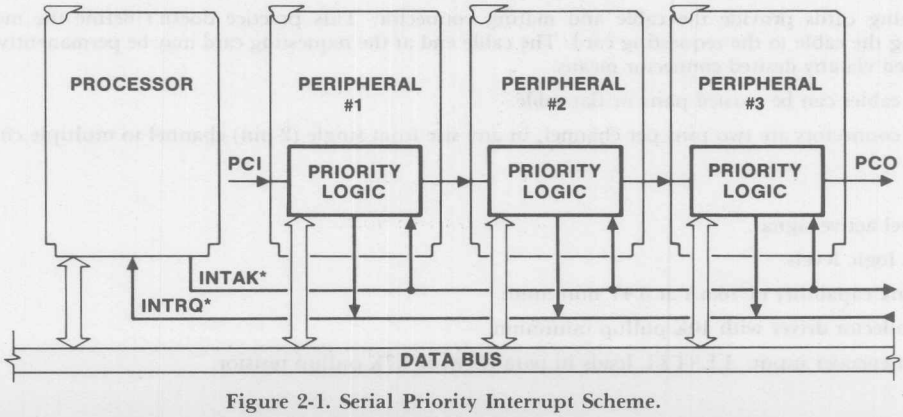


Figure 2-1. Serial Priority Interrupt Scheme.

Parallel Priority. A parallel priority scheme can be implemented on the STD BUS, so that the priority logic rides on a separate card and not on each peripheral card. The parallel priority card is a modular function that can be tailored to individual processor requirements. This scheme allows peripheral cards to be processor-independent. It requires that the individual requests and acknowledges be made from the user edge of the card, as shown in Figure 2-2.

Note that a difference exists between an interrupt priority encoder and a bus priority decoder. The interrupt encoder doesn t need to send an acknowledge back to the requesting peripheral. The processor simply begins to service the interrupting device through normal bus operations. A bus priority decoder must decode the acknowledge back to the requesting peripheral, so that it knows when to take control of the bus.

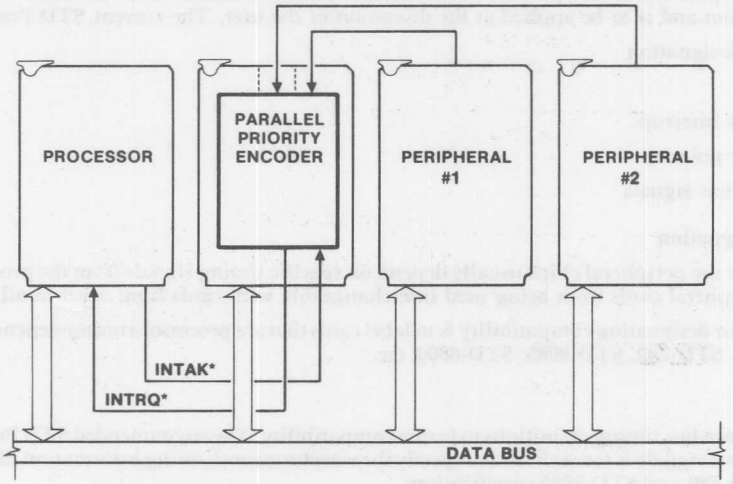


Figure 2-2. Parallel Priority Interrupt Scheme.

STD Practice for Parallel Priority Interrupt. Cards designed to work with the parallel priority scheme require circuit connections at the user interface edge of the card. The STD Practice for compatibility is:

Mechanical:

- Two connections for each request channel: a request signal and a ground signal.
- Connector layout for priority encoder cards as shown in Figure 2-3. The ground pins are the top row and the request pins are the bottom row.
- Connector pins are 0.025-in. square posts or equivalent.
- Requesting cards provide the cable and mating connector. This practice doesn't define the method for fastening the cable to the requesting card. The cable end at the requesting card may be permanently wired or connected via any desired connector means.
- Mating cables can be twisted pairs or flat cable.
- Mating connectors are two pins per channel, in any size from single (2-pin) channel to multiple channel.

Electrical:

- Low-level active signal.
- LSTTL logic levels.
- Drive sink capability of 16mA at 0.4V minimum.
- Open-collector driver with 10K pullup minimum.
- Load on encoder input: 4 LSTTL loads in parallel with 4.7K pullup resistor.

Pullup resistors on the encoder card inputs are recommended to disable the request if no connection is made. Open-collector drivers on requesting cards are recommended, to allow wire-ORing of multiple requests on a single channel. This scheme is useful for low-level requests and requires the processor to poll to identify the requester.

The implementation of the parallel priority interrupt on the STD BUS is shown in Figure 2-4.

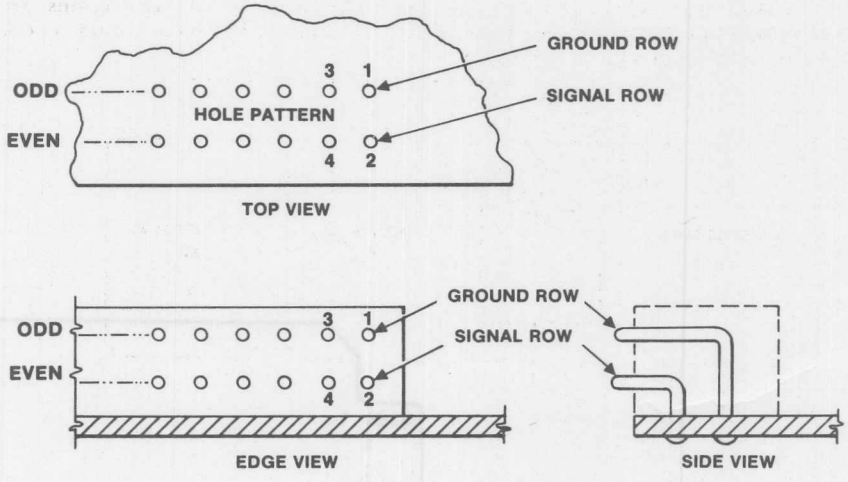


Figure 2-3. Recommended Connector Arrangement for Priority Encoder Cards.

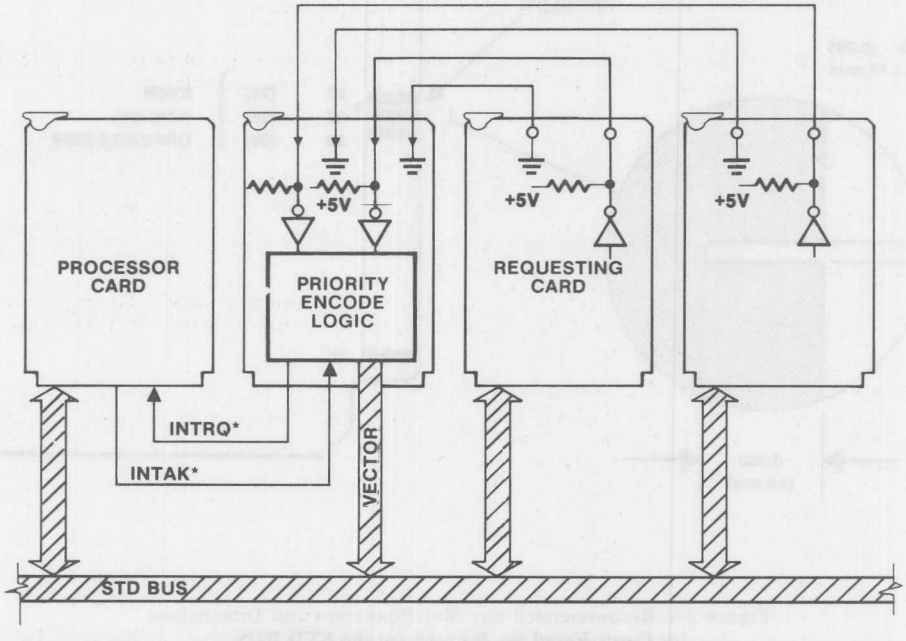


Figure 2-4. Recommended Implementation of Parallel Priority Interrupt on the STD BUS.

Card Keying for Polarity

Upside-down card insertion can be prevented with a single, offset key slot. The slot is located between pins 25 and 27, and between 26 and 28, for cards keyed for polarity (Fig. 2-5).

Cards keyed for **position** must not use the slot between pins 27 and 29 or between 28 and 30, as this would invalidate the polarity keying.

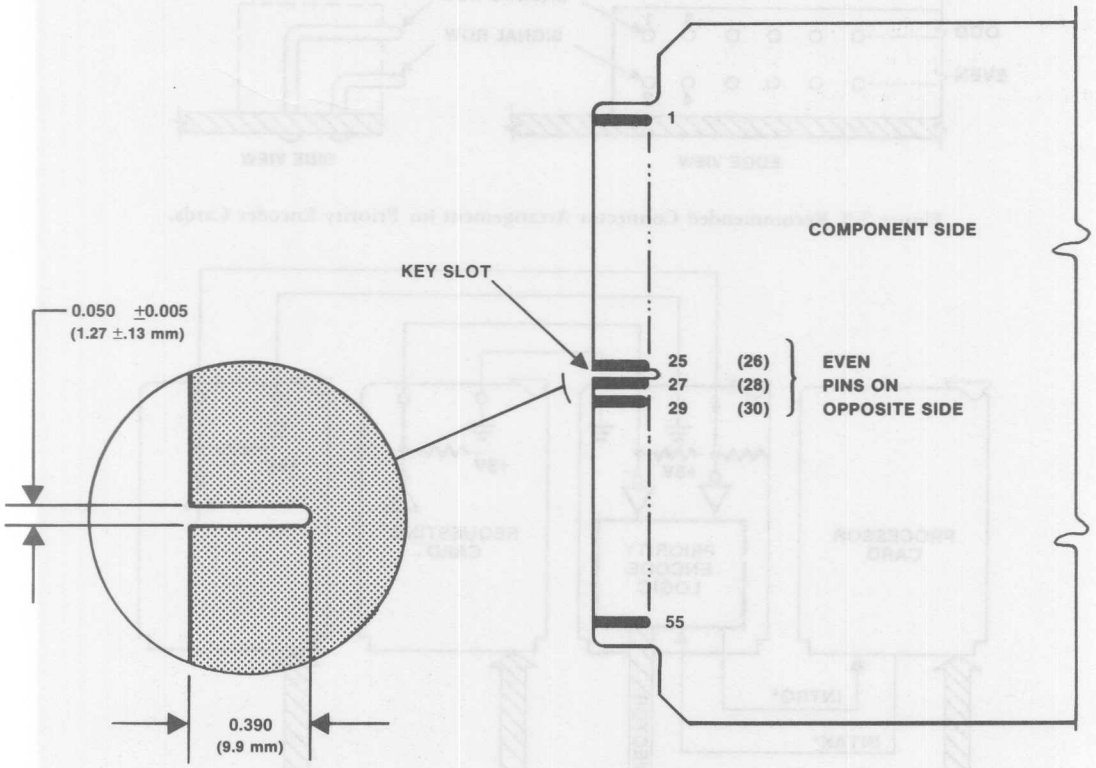


Figure 2-5. Recommended Key Slot Placement and Dimensions for Cards Keyed for Polarity on the STD BUS.

Open-Collector Bus Signals

Bus control inputs to the processor card are often wire-OR connected, which requires open-collector drivers. It is recommended, as STD Practice, that the following signals be open-collector on any source card and pulled-up on any destination card:

- BUSRQ* —Pin 42
- INTRQ* —Pin 44
- WAITRQ* —Pin 45
- NMIRQ* —Pin 46
- SYSRESET* —PIN 47
- PBRESET* —PIN 48

Also, it is recommended that these lines be specified as follows:

- Low-level active signal
- LSTTL logic levels
- Driver sink capability of 16mA at 0.4V
- Open-collector driver with 10K pullup
- Destination load pullup of 4.7K

SECTION 3
STD 7000 Specifications

Introduction

Series 7000 comprises a wide range of modular microprocessor system elements, including processor, memory cards, I/O cards, motherboards, card racks, utility cards, and power supplies, which provide high functional density with the design options needed for efficient system partitioning. The cards are divided into the following categories:

7100 System support cards [(non-4.5 x 6.5 in. (114.30 x 165.10 mm)] including motherboards
7300 Peripheral interface
7400 Analog I/O
7500 Industrial I/O
7600 Digital (TTL) I/O
7700 Memory
7800 Processors
7900 Utility (extenders, blanks, prototyping aids, etc.)

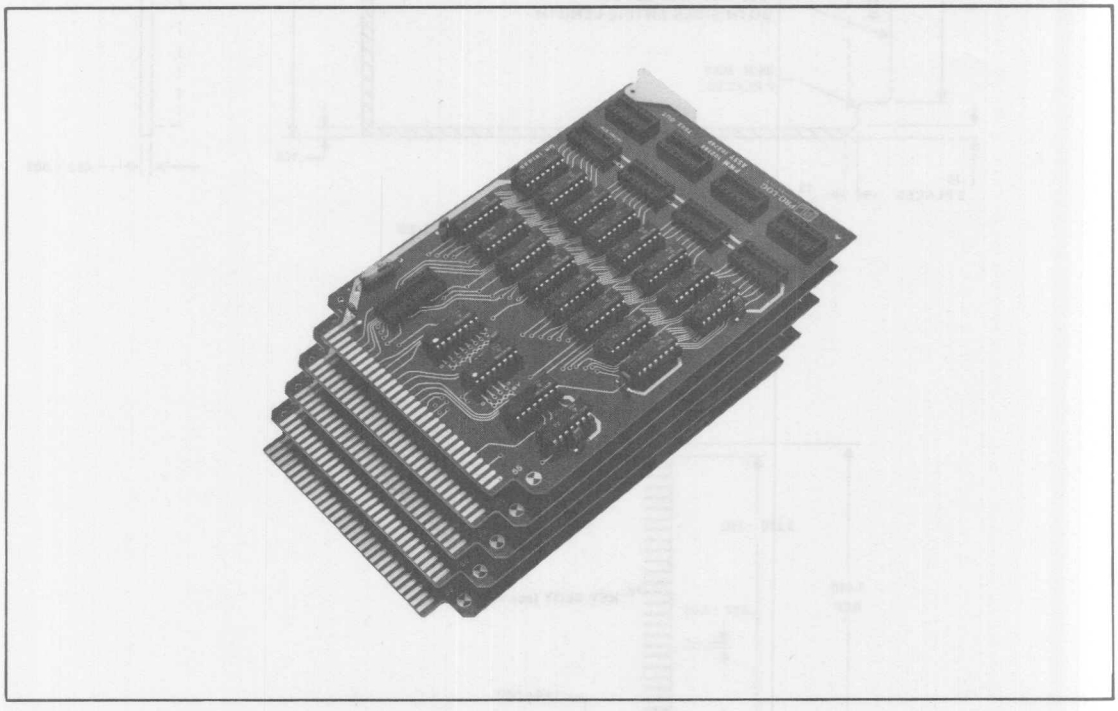


Figure 3-1. STD 7000 Family.

This section contains specifications common to the Series 7000 cards. These specifications, combined with the STD BUS specifications and the user's manuals of the individual cards, fully specify each card. Configuring the hardware for a Series 7000 STD BUS system simply requires the defining of the memory size and the number and type of I/O lines needed for the application, together with the selection of the appropriate card rack and special cards. Mapping of the memory and I/O is preassigned; changes may be incorporated by moving jumper wires.

Mechanical Specifications

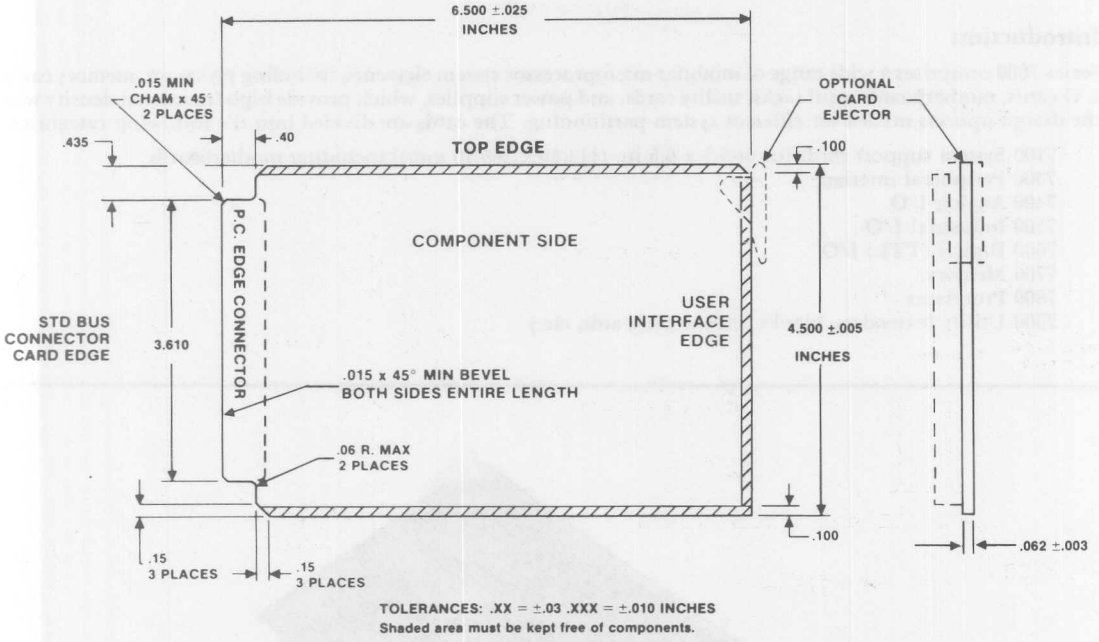


Figure 3-2. STD BUS Card Outline - Inches.

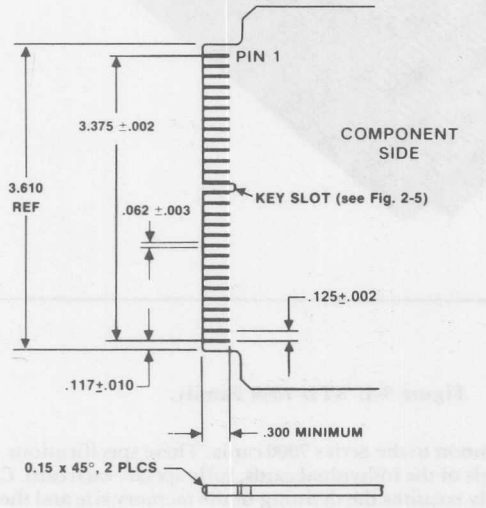


Figure 3-3. STD BUS Edge Card Finger Design - Inches.

Mechanical Specifications

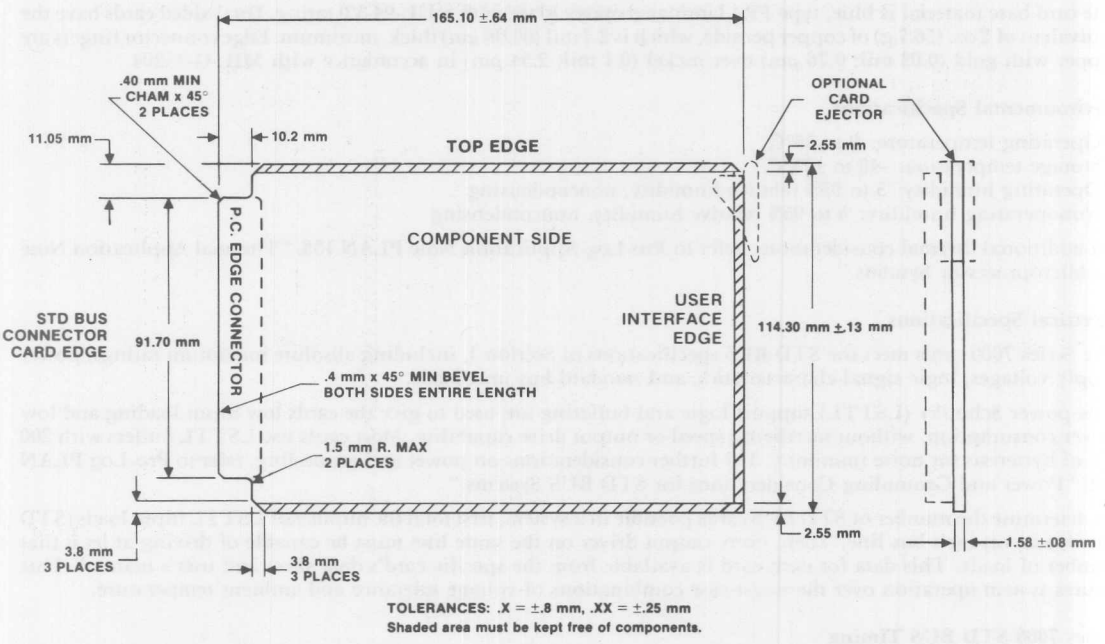


Figure 3-5. STD BUS Edge Card Finger Design - Metric.

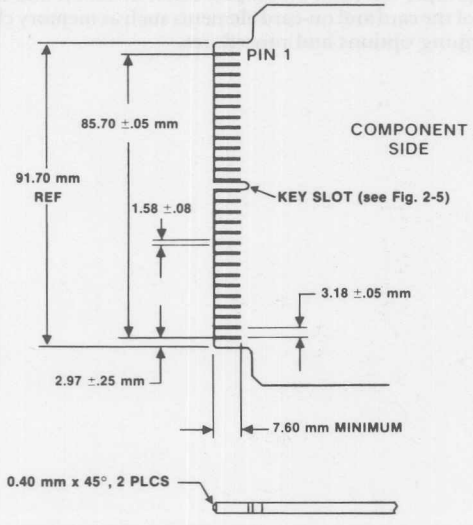


Figure 3-4. STD BUS Card Outline - Metric

STD 7000 SPECIFICATIONS

Materials

The card base material is blue, type FR4 laminated epoxy glaze with a UL-94-V0 rating. Dual-sided cards have the equivalent of 2 oz. (56.7 g) of copper per side, which is 2.4 mil (60.96 μm) thick, minimum. Edge connector fingers are copper with gold (0.03 mil; 0.76 μm) over nickel (0.1 mil; 2.54 μm) in accordance with MIL-G-45204.

Environmental Specifications

- Operating temperature: 0 to 55°C
- Storage temperature: -40 to +75°C
- Operating humidity: 5 to 95% relative humidity, noncondensing
- Nonoperating humidity: 5 to 95% relative humidity, noncondensing

For additional thermal considerations, refer to Pro-Log Application Note PLAN 133, "Thermal Application Note for Microprocessor Systems."

Electrical Specifications

The Series 7000 cards meet the STD BUS specifications of Section 1, including absolute maximum ratings, power supply voltages, logic signal characteristics, and standard bus unit loads.

Low-power Schottky (LSTTL) support logic and buffering are used to give the cards low input loading and low power consumption, without sacrificing speed or output drive capability. Most cards use LSTTL buffers with 200 mV of hysteresis for noise immunity. For further considerations on power and grounding, refer to Pro-Log PLAN 134, "Power and Grounding Considerations for STD BUS Systems."

To determine the number of STD BUS cards possible in a system, first total the number of LSTTL input loads (STD unit loads) on each bus line. Then, every output driver on the same line must be capable of driving at least that number of loads. This data for each card is available from the specific card's data sheet and user's manual. This assures system operation over the worst-case combinations of voltage tolerance and ambient temperature.

Series 7000 STD BUS Timing

For card timing information, refer to the individual data sheets and user's manuals.

Card Addressing Options

User addressing options are made by a jumper selection on all processor, memory, and I/O cards, which allow the user to permanently change the address of the card and on-card elements such as memory chips and ports. Refer to the user's manuals for specific address mapping options and procedures.

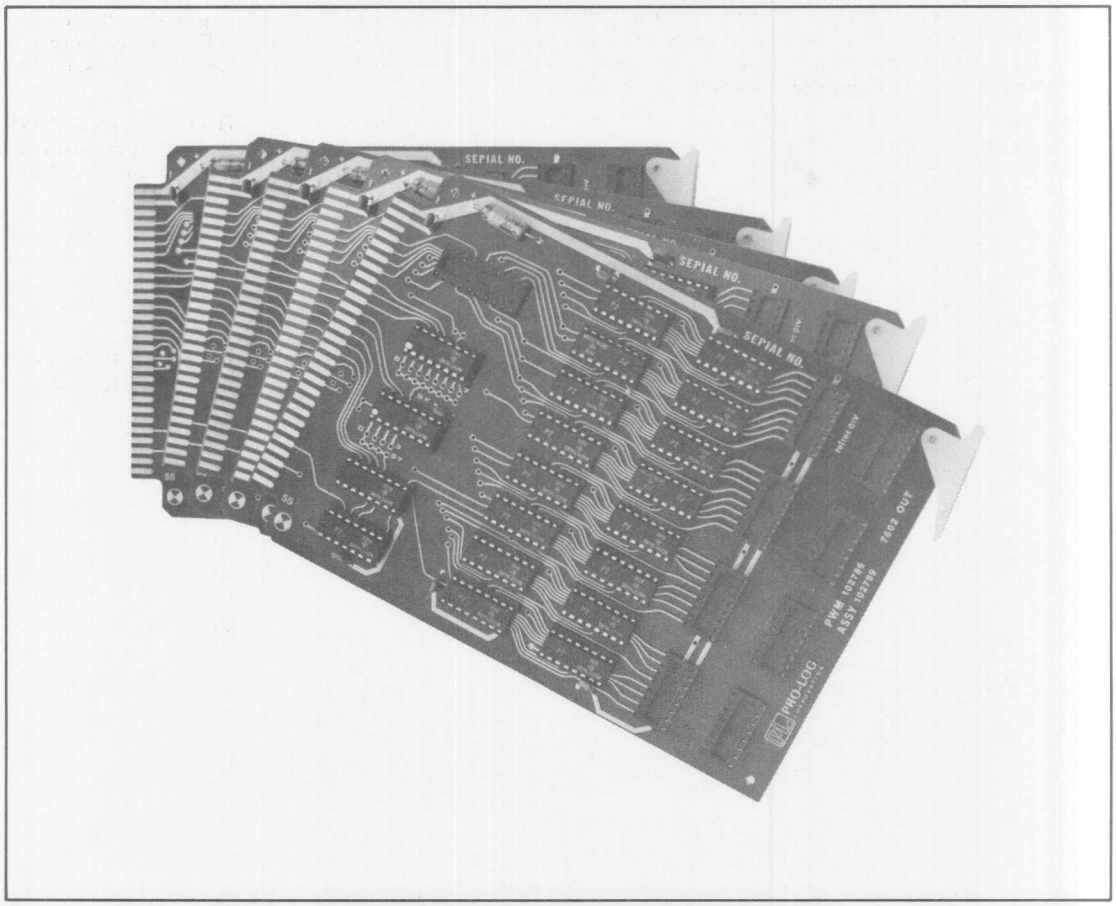
SECTION 4
Series 7000 Data Sheets

INTRODUCTION

This catalog contains STD 7000 data sheets that give additional specifications and operating requirements for specific STD 7000 cards and accessories.

For convenience, the data sheets of the STD 7000 cards are arranged by function in the following sequence:

7100 System Support Cards [non - 4.5 x 6.5 in. (11.43 x 16.51 cm)]
7300 Peripheral Interface
7500 Industrial I/O
7600 Digital (TTL) I/O
7700 Memory
7800 Processors
7900 Utility (extenders, blanks, etc.)
— Miscellaneous Accessories



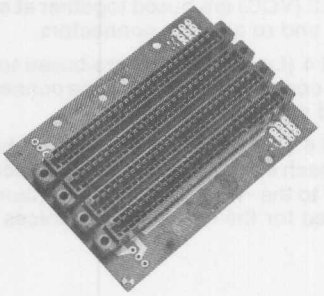
7000 STD BUS

7101, 7102, & 7105 MOTHERBOARDS

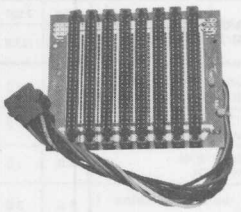
The Series 7100 Motherboards implement the STD BUS backplane interconnection scheme as defined by the STD BUS general specifications. They are available as single units, or as an integral part of the preassembled STD BUS card racks.

FEATURES

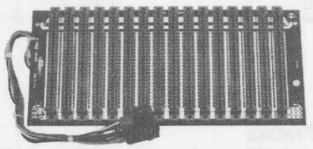
- **56-pin edge connectors on 0.5 in. (12.7 mm) centers, with interconnect wiring for STD BUS microprocessor systems**
- **High current power distribution and logic bus traces**
- **Groundplane for reduced crosstalk and noise**
- **Supplied with power cable and 9-pin keyed connector**
- **Four edge connectors (7105)**
- **Eight edge connectors (7101)**
- **Sixteen edge connectors (7102)**
- **Universal processor compatibility—Z80, 8085, 6800, and others.**



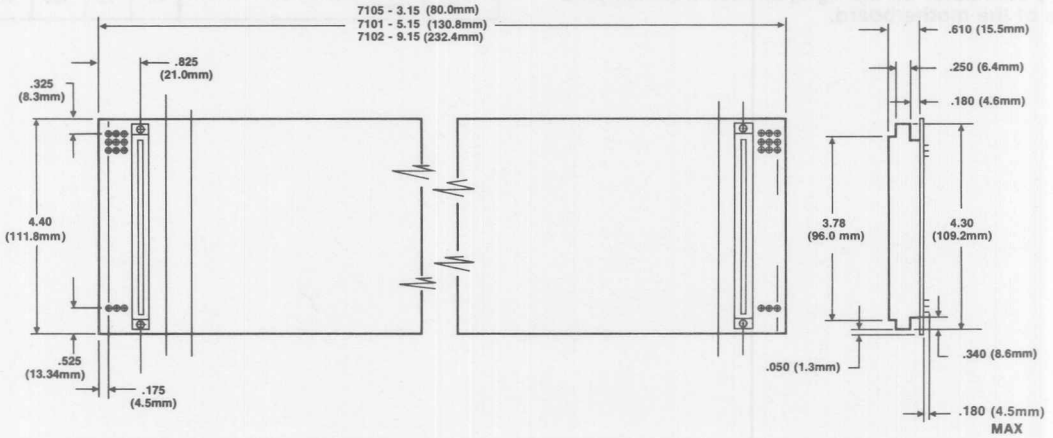
7105



7101



7102



FUNCTIONAL/ELECTRICAL

Digital Power Traces

Pins 1 and 2 (VCC) are bused together at each edge connector and to all edge connectors.

Pins 3 and 4 (Logic Ground) are bused together at each edge connector and to all edge connectors and the ground plane.

Pins 5 and 6 (-VBB) are separaged and bused pin-for-pin to each edge connector. These traces are not connected to the -VBB power harness. Jumper pads are provided for the connection of traces to -VBB.

SYMBOL	PARAMETER FOR TOTAL MOTHERBOARD	7105 MAX	7101 MAX	7102 MAX	UNITS
I_{VCC}	VCC trace current (Pins 1 and 2) (10°C rise from 20°C)	17.0	17.0	17.0	A
I_{LG}	Logic ground trace (pins 3 and 4) (10°C rise from 20°C)	17.0	17.0	17.0	A
I_{BB}	VBB current (pin 5 or 6) (10°C rise from 20°C)	1.0	1.0	1.0	A
R_{VCC}	VCC trace resistance (pins 1 and 2) at 20°C	1.5	3.0	6.0	mΩ
R_{LG}	Logic ground trace resistance (pins 3 and 4) at 20°C	1.5	3.0	6.0	mΩ
R_{BB}	VBB trace resistance (pin 5 or 6) at 20°C	68.0	135.0	270.0	mΩ

Logic Bus Traces

Pins 7 through 50 are bused pin-for-pin to all edge connectors. Pins 51 and 52 (PC0) and PC1) are open across each edge connector, with pin 52 on each edge connector connected to pin 51 on the adjacent edge connector on the right, as seen from the card side of the motherboard.

SYMBOL	PARAMETER FOR TOTAL MOTHERBOARD	7105 MAX	7101 MAX	7102 MAX	UNITS
I_{LT}	Logic trace current (10°C rise from 20°C)	1.0	1.0	1.0	A
C_{LL}	Logic trace to logic trace capacitance (measured at 1.0 MHz)	7.0	13.0	25.0	pF
C_{LG}	Logic trace to logic ground capacitance (measured at 1.0 MHz)	13.0	25.0	50.0	pF
R_{LT}	Logic trace resistance at 20°C	68.0	135	270	mΩ

Auxiliary Power Traces

Pin 55 (AUX +V) and pin 56 (AUX -V) are bused pin-for-pin to all edge connectors.

User's Manuals

To obtain the user's manual for the 7101, 7102, and 7105 motherboards, ask for Pro-Log document #106418.

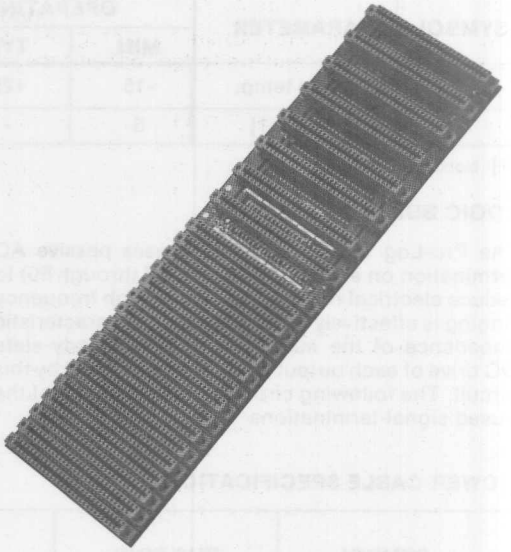
Pins 53 and 54 (AUXGND) are bused together at each card edge connector and to all edge connectors.

SYMBOL	PARAMETER FOR TOTAL MOTHERBOARD	7105 MAX	7101 MAX	7102 MAX	UNITS
I_{A+}	Analog V+ trace current (10°C rise from 20°C)	7.0	7.0	7.0	A
I_{A-}	Analog V- trace current (10°C rise from 20°C)	7.0	7.0	7.0	A
I_{AG}	Analog ground trace current (10°C rise from 20°C)	12.0	12.0	12.0	A
R_{A+}	Analog V+ trace resistance at 20°C	4.0	7.5	15.0	mΩ
R_{A}	Analog V- trace resistance at 20°C	4.0	7.5	15.0	mΩ
R_{AG}	Analog ground trace resistance at 20°C	4.0	7.5	15.0	mΩ

7000 STD BUS

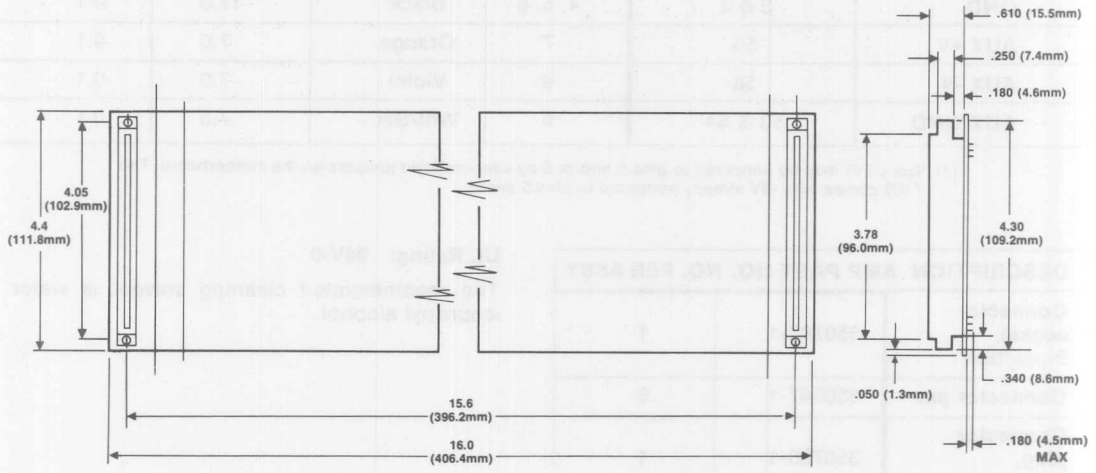
7106 MOTHERBOARD

The 7106 motherboard implements the STD BUS backplane interconnection scheme as defined by the STD BUS general specification. It is available as a single unit, or as an integral part of the preassembled STD BUS card racks. A power supply cable with locking nine-pin connector is included.



FEATURES

- **56-pin edge connectors on 0.5 in. (12.7 mm) centers, with interconnect wiring for STD BUS microprocessor systems**
- **16 card slots on 0.5 in. (12.7 mm) centers**
- **8 card slots on 1-in. (25.4 mm) centers**
- **Accepts all STD BUS cards**
- **High current power distribution and logic bus traces**
- **Groundplane for reduced crosstalk and noise**
- **Power-supply cable included**
- **Passive AC terminations**
- **Supplied with power cable and 9-pin keyed connector**



*Diminsions for reference only.
Consult users manual for details.

7106 MOTHERBOARD

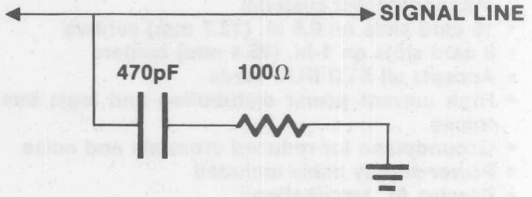
ENVIRONMENTAL SPECIFICATIONS

SYMBOL	PARAMETER	RECOMMENDED OPERATING LIMITS			ABSOLUTE NONOPERATING LIMITS		
		MIN	TYP	MAX	MIN	MAX	UNIT
T_A	Free air temp.	-15	+25	+85	-15	+85	°C
—	Humidity [1]	5	-	95	5	95	%RH

[1] Noncondensing

LOGIC BUS TERMINATION

The Pro-Log 7106 motherboard uses passive AC termination on all signal lines (pins 7 through 50) to reduce electrical ringing. Undesired high frequency ringing is effectively terminated to the characteristic impedance of the motherboard. The steady-state DC drive of each output driver is not reduced by this circuit. The following circuit represents each of the bused signal terminations



POWER CABLE SPECIFICATIONS

SYMBOL	BUS PINS	POWER CABLE		RECOMMENDED CURRENT (A)	
		PINS	COLOR	MAX	MIN
V_{cc}	1 & 2	1 & 2	Red	17.0	0.1
V_{bb}	5 [1]	3	White	1.0	0.1
V_{bb}	6 [1]	3	White	1.0	0.1
GND	3 & 4	4, 5, 6	Black	17.0	0.1
AUX +V	55	7	Orange	7.0	0.1
AUX -V	56	9	Violet	7.0	0.1
AUX GND	53 & 54	8	Wht/Blk	7.0	0.1

[1] V_{bb} (-5V) may be jumpered to pins 5 and/or 6 by user-installed jumpers on the motherboard. The 7106 comes with -5V already jumpered to pins 5 and 6.

DESCRIPTION	AMP PART NO.	NO. PER ASSY
Connector socket, 9-position	350782-1	1
Connector pin	350547-1	9
Connector plug, 9-position	350720-1	1
Contact socket	350550-1	9

Source for Connectors - AMP, INC.

UL Rating: 94V-0

The recommended cleaning solvent is water or isopropyl alcohol.

USER's MANUAL

To obtain the user's manual for the 7106, ask for Pro-Log document #106998.

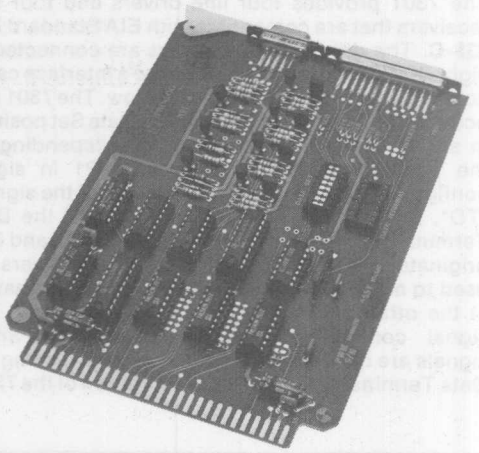
7000 STD BUS

7301 RS-232 & TTY DRV/REC CARD

The 7301 combines the I/O ports and the voltage translation needed to interface a microprocessor to RS-232-C and TTY serial data communications lines. The RS-232-C and TTY circuits feature separate control ports for programming convenience, and cable interlocks that can be tested. The microprocessor card used in conjunction with the 7301 is programmed to provide timing and serial/parallel conversion for both interface circuits.

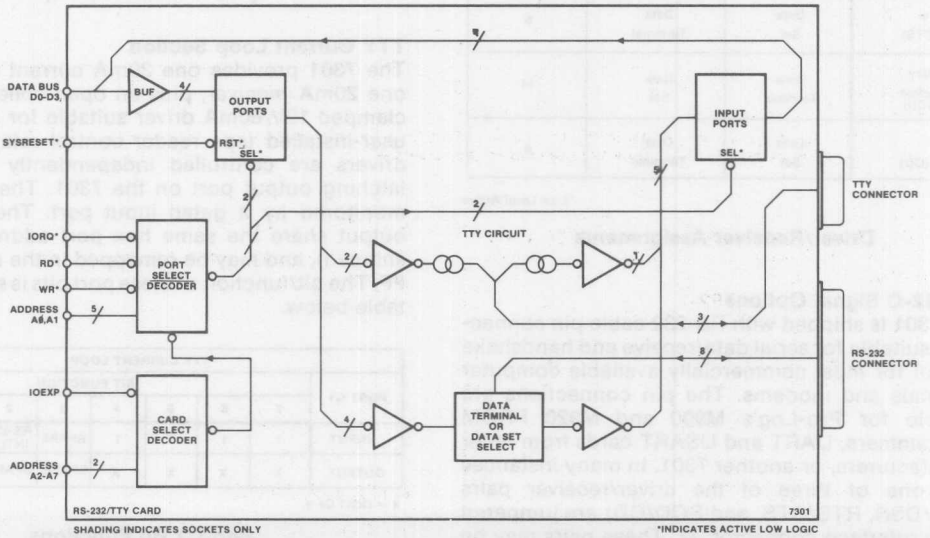
The RS-232-C section of the 7301 provides four line drivers and four line receivers (which are compatible with EIA Standard RS-232-C), and a 25-pin D-type cable connector. A pair of DIP sockets on the card enables user-selected Data Terminal or Data Set (modem) configurations by simply inserting a shorting plug (included) into one of the sockets. Operating speed ranges between 0 - 20,000 baud.

The TTY section of the 7301 consists of separate send and receive 20mA current loops, a relay driver for remote control of an ASR-33 type console tape reader, and a 9-pin D-type cable connector. Operating speed ranges between 0 - 300 baud.



FEATURES

- **EIA RS-232-C Compatible Interface**
- **ASR/KSR TTY Interface**
- **Simultaneous Full Duplex Operation**
- **On-card Industry Standard Cable Connectors**
- **Program Readable Cable Interlocks**
- **User-selectable Data Terminal/Data Set Configuration**
- **User-selectable Port Addresses**
- **System Processor Generated Baud Rate**
- **Universal Processor Compatability - Z80, 8085, 6800, and others.**



7301 RS-232 & TTY DRIVER/RECEIVER CARD

FUNCTIONAL

RS-232-C Section

The 7301 provides four line drivers and four line receivers that are compatible with EIA Standard RS-232-C. The drivers and receivers are connected to eight RS-232 signal pins at the card's interface cable connector as shown in the table below. The 7301 can occupy either the Data Terminal or Data Set position in an RS-232 communications link, depending on the position of the shorting plug P1 in signal configuration sockets J3 and J4. Four of the signals (TD*, DTR, RTS, and SCD) originate at the Data Terminal, and four signals (RD*, DSR, CTS, and CD) originate at the Data Set. The four line receivers are used to monitor complementary signals originating at the other end of the communications link. The signal configuration sockets determine which signals are driven or received, thus establishing the Data Terminal or Data Set configuration of the 7301.

RS-232 SIGNAL	DRIVER AT	RECEIVER AT	7301 J2 PIN
Transmitted Data (TD*)	Data Terminal	Data Set	2
Received Data (RD*)	Data Set	Data Terminal	3
Data Terminal Ready (DTR)	Data Terminal	Data Set	20
Data Set Ready (DSR)	Data Set	Data Terminal	6
Request To Send (RTS)	Data Terminal	Data Set	4
Clear To Send (CTS)	Data Set	Data Terminal	5
Secondary Transmitted Data (SCD)	Data Terminal	Data Set	14
Carrier Detect (CD)	Data Set	Data Terminal	8

*Low Level Active

Driver/Receiver Assignments

RS-232-C Signal Options

The 7301 is shipped with RS-232 cable pin connections suitable for serial data/receive and handshake control for most commercially available computer terminals and modems. The pin connections are suitable for Pro-Log's M900 and M920 PROM Programmers, UART and USART cards from other manufacturers, or another 7301. In many instances only one of three of the driver/receiver pairs (DTR/DSR, RTS/CTS, and SCD/CD) are jumpered to the interface connector J2. These pairs may be rejumpered to other J2 pins as required in the application. Pads are provided on the card for rejumpering undriven pins to positive and negative DC supplies as permanent signals when needed.

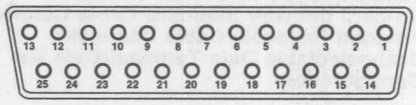
The RS-232 drivers are controlled independently by a 4-bit latching output port on the 7301. The RS-232 receivers are monitored by a 4-bit latching input port. **The input and output ports share the same hex port address (C0 as shipped), and may be remapped in the range of 00-FF.** The input and output ports communicate with a processor card over the four least significant bits of the STD data bus.

DATA TERMINAL CONFIGURATION								
PORT C0	BIT FUNCTION							
	7	6	5	4	3	2	1	0
INPUT (RECEIVERS)	1	1	1	1	DSR	CD	CTS	RD
OUTPUT (DRIVERS)	X	X	X	X	DTR	SCD	RTS	TD

DATA SET CONFIGURATION								
PORT C0	BIT FUNCTION							
	7	6	5	4	3	2	1	0
INPUT (RECEIVERS)	1	1	1	1	DTR	SCD	RTS	TD
OUTPUT (DRIVERS)	X	X	X	X	DSR	CD	CTS	RD

X = Don't Care

Port CO Bit Functions



RS-232 Connector Pins, Female (7301 J2 Front View)

TTY Current Loop Section

The 7301 provides one 20mA current loop driver; one 20mA receiver; plus an open-collector diode-clamped 12V/60mA driver suitable for switching a user-installed tape reader control relay. The TTY drivers are controlled independently by a 4-bit latching output port on the 7301. The receiver is monitored by a gated input port. The input and output share the same hex port address. (C1 as shipped), and may be remapped in the range of 00-FF. The bit/function of these port bits is shown in the table below.

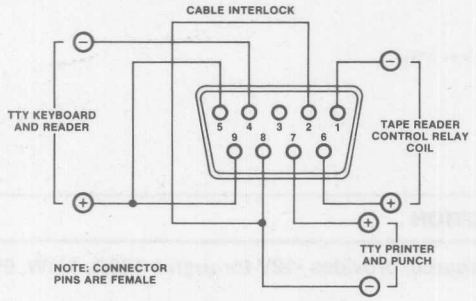
TTY CURRENT LOOP								
PORT C1	BIT FUNCTION							
	7	6	5	4	3	2	1	0
INPUT	1	1	1	1	SPARE	RS-232 INTLK	TTY INTLK	DATA IN
OUTPUT	X	X	X	X	SPARE	SPARE	TAPE CTRL	DATA OUT

X = Don't Care

* Low Level Active

Port C1 Bit Functions

FUNCTIONAL (continued)



Recommended TTY Hookup (J1 Front View)

Common Features

The RS-232 cable connection on the 7301 is made by an industry standard 25-pin D-type connector. The TTY connector is a 9-pin D type. Both connectors are located below the card ejector and each includes an input port pin for a user-added cable interlock. These are used by connecting the pins (shown in the pin lists) to signal ground in the cable assembly.

The SYSRESET* input to the 7301 clears both the RS-232 and TTY output ports, resulting in STOP bits on the RS-232 and TTY serial data lines, TTY tape reader off, and inactive RS-232 control signals. SYSRESET* has no effect on the gated input ports.

Card Address Mapping

The 7301 card is selected by a decoded combination of address lines A1-A7. The user chooses the card address combination by connecting each jumper wire from SC, SY, SZA, and SZB to pad matrices adjacent to U2, U3, U4, and U5. The 7301 is shipped with hex port addresses C0 (RS-232) and C1 (TTY) connected. To map the 7301 anywhere in the hex port address range 00-FF, change the decoder output jumpers. For additional information, see *User's Manual.*

Port address line A0 selects one of the two sequential port addresses to use either the RS-232 or TTY circuits. One input port and one output port (4 bits only) reside at each address on the 7301. The RD* and WR* control inputs differentialte between input gating and output latch functions.

*Low Level Active

ELECTRICAL

- VCC = +5V, ±5%
- ICC = 525mA maximum (380mA typical)
- AUX -V = -12V ±5%
- AUX I = -200mA maximum
- Address, data, and control buses meet all STD BUS general electrical specifications.

SYMBOL	PARAMETER	MIN	MAX	UNIT	NOTE
VOH	High Level Output Voltage	+3		V	1
VOL	Low Level Output Voltage	-3		V	
IOS	Output Short Circuit Current, Output Shorted To ±12V (Duration 1 Second Maximum)		85	mA	
CL	Output Load Capacitance		2500	pF	2
Tr Tf	Output Rate of Change		30	V/μs	
VIH	Input High Level Voltage	+3	+25	V	3
VIL	Input Low Level Voltage	-25	-3	V	
IIH	Input High Level Current	+0.5	+8.5	mA	
IIL	Input Low Level Current	-8.5	-0.5	mA	
EL	Output Termination Bias	-2.0	+2.0	V	
	BAUD Rate (Bits/Second)	0	20,000	Baud	
	Recommended Cable Length		50 16	ft m	
VO	Driver Open Circuit Output Voltage	-12	+5	V	
RO	Driver Output Resistance, Power Off	300		Ω	
RL	Input Load Resistance	3K	6K	Ω	3

NOTES: 1. Minimum load resistance 3KΩ. 2. Includes cable and terminator capacitance. 3. Except Cable Interlock, which is 4 LSTTL input loads.

7301 RS-232 Connector J2

ELECTRICAL (continued)

J1 PIN	FUNCTION
1	Paper-tape motion control, relay coil power source; provides -12V through a 100Ω, 1/4W, 5% resistor (diode clamp to pin 6)
2	Interface cable interlock input; active low logic; use is optional. Designed to be connected to logic ground (pin 8) by the interface cable when the cable is plugged into 7301 J1. Read into the processor as input port C1 bit 1; a logic 1 is returned when pin 2 is grounded, or a logic 0 when open. Input loading 4 LSTTL loads.
3	Spare pin; connected to a pad on the 7301 adjacent to pads supplying +5V or -12V. User may connect a jumper wire or a 1/2W resistor to either voltage for special applications.
4	Current loop return (7301 receive); supplies -12V through a 470Ω, 1/2W, 5% resistor supplying 20 mA return and pin-9 voltage pulldown when the TY commutator is closed (spacing). Not required in some instrument interfaces.
5	20 mA source (7301 receive); supplies +20 mA from +5V through a 220Ω, 1/4W, 5% resistor when the TTY commutator is closed (spacing) and pulls up pin 9 when the commutator is open (marking).
6	Paper-tape control relay drive; supplies up to +50 mA through a switching transistor and 100 Ω, 1/4W, 5% resistor when output port C1 bit 1 is at logic 1 (+5V current source). When output port C1 bit 1 is at logic 0 or the 7301 is reset, output leakage current is 0. 1 mA maximum (pin 6 at 0V).
7	20 mA source (7301 transmit); provides +20 mA minimum (measured with pin 7 at 0V) from the +5V supply through a switching transistor and a 200Ω, 1/4W, 5% resistor when output port C1 bit 0 is at logic 0. Output leakage current (pin 7 at OV) with output port C1 bit 0 at logic 1 is 0.1 mA maximum. Note that this output supplies +20 mA when the 7301 is reset. Pads are provided for jumpering across the 200Ω resistor in instrument interface applications requiring additional drive voltage.
8	Logic ground out; connects to LOGIC GROUND (STD BUS pins 3,4).
9	Current Loop Receive (7301 receive); a transistor base input through a 4.7KΩ, 1/4W, 5% resistor and negative current clamp diode. A voltage greater than +2.5V applied to pin 9 is returned to the processor as input port C1 bit 0 at logic 1. A voltage lower than +0.8V is read as logic 0.

J1 Current Loop Connector Specifications

MECHANICAL

Meets all STD BUS general mechanical specifications except for the RS-232-C and TTY connectors, which protrude from the card front 0.375-in. (9.53 mm), and except for card width, which may require two card slots for cable connector clearance on the card wiring side. See figure below.

TTY CONNECTOR PIN LIST					
PIN NUMBER	SIGNAL FLOW		PIN NUMBER	SIGNAL FLOW	
SIGNAL					SIGNAL
-12V/100Ω SOURCE	OUT	1	6	OUT	SWITCHED RELAY SINK*
CABLE INTERLOCK*	IN	2	7	OUT	CURRENT LOOP TRANS*
(SPARE)		3	8	OUT	LOGIC GROUND
-12V/470Ω SOURCE	OUT	4	9	IN	CURRENT LOOP RECV*
+5V/220Ω SOURCE	OUT	5			

*Designates Active Low Level Logic

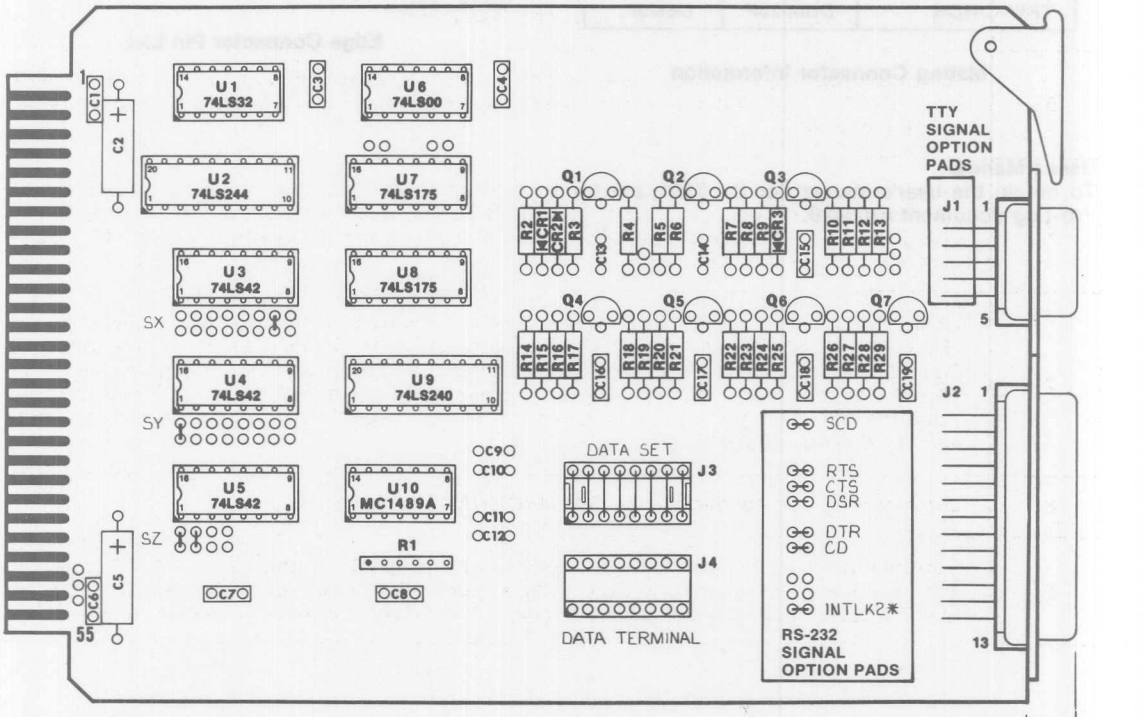
TTY Connector Pin List

RS-232 CONNECTOR PIN LIST					
PIN NUMBER	SIGNAL ORIGIN		PIN NUMBER	SIGNAL ORIGIN	
SIGNAL					SIGNAL
PROTECTIVE GROUND		1	14	T□	SEC. TRANSMITTED DATA*
TRANSMITTED DATA*	T■	2	15	S	TRANS SIGNAL TIMING
RECEIVED DATA*	S■	3	16	S	SEC. RECEIVED DATA*
REQUEST TO SEND	T□	4	17	S	RECV. SIGNAL TIMING
CLEAR TO SEND	S□	5	18		(UNASSIGNED)
DATA SET READY	S□	6	19	T	SEC. REQUEST TO SEND
SIGNAL GROUND	OUT	7	20	T□	DATA TERMINAL READY
CARRIER DETECT	S□	8	21	S	SIGNAL QUALITY DETECT
(TEST)		9	22	S	RING INDICATOR
(TEST)		10	23	T/S	DATA SIGNAL RATE SEL.
(UNASSIGNED)		11	24	T	TRANS. SIGNAL TIMING
SEC. CARRIER DETECT	S	12	25	IN□	CABLE INTERLOCK*
SEC. CLEAR TO SEND	S	13			

*Designates Active Low Level Logic

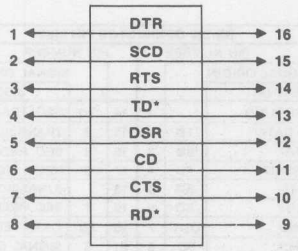
LEGEND:
T - Signal Originates At Data Terminal (DTE)
S - Signal Originates At Data Set (DCE)
■ - Permanent Connection On 7301
□ - Jumper Connection On 7301; May Be Relocated By User

RS-232 Connector Pin List



7301 User Options

7301 RS-232 & TTY DRIVER/RECEIVER CARD



Data Terminal/Data Set Select Plug P1 Wiring
(Shorting Bars Exposed for Scope Test Points)

MANUFACTURER	CONNECTOR MODEL	
	RS-232-C (25-PIN D)	TTY (9-PIN D)
AMPHENOL	17-90250-16	17-90090-16
ITT-CANNON	DBM-25P	DEM-9P
TRW-CINCH	DBM-25P	DEM9P

Mating Connector Information

User's Manual
To obtain the user's manual for the 7301, ask for Pro-Log document #106420.

STD 7301 EDGE CONNECTOR PIN LIST							
PIN NUMBER				PIN NUMBER			
OUTPUT (LSTTL DRIVE)						OUTPUT (LSTTL DRIVE)	
INPUT (LSTTL LOADS)						INPUT (LSTTL LOADS)	
MNEMONIC							MNEMONIC
+5 V	IN		2	1		IN	+5 V
GROUND	IN		4	3		IN	GROUND
-5V			6	5			-5V
D7			8	7	55	1	D3
D6			10	9	55	1	D2
D5			12	11	55	1	D1
D4			14	13	55	1	D0
A15			16	15		1	A7
A14			18	17		1	A6
A13			20	19		1	A5
A12			22	21		1	A4
A11			24	23		1	A3
A10			26	25		1	A2
A9			28	27		1	A1
A8			30	29		1	A0
RD*	1		32	31		1	WR*
MEMRQ*			34	33		1	IORQ*
MEMEX			36	35		1	IOEXP
MCSYNC*			38	37			REFRESH*
STATUS 0*			40	39			STATUS 1*
BUSRQ*			42	41			BUSAK*
INTRQ*			44	43			INTAK*
NMIRQ*			46	45			WAITRQ*
PBRESET*			48	47		1	SYSRESET*
CNTRL*			50	49			CLOCK*
PCI	IN		52	51	OUT		PCO
AUX GND	IN		54	53	IN		AUX GND
AUX -V (-12V)	IN		56	55			AUX +V

*Active low level logic

Edge Connector Pin List

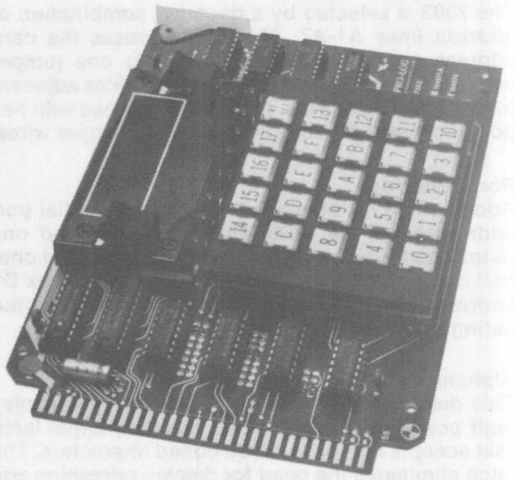
7000 STD BUS

7303 KEYBOARD DISPLAY CARD

The 7303 is a general purpose, control panel card that provides data input and display capability. The card includes an 8-position alphanumeric display keyboard with 24 program-definable keys plus system reset, an 8-bit binary LED display, and two rocker switches.

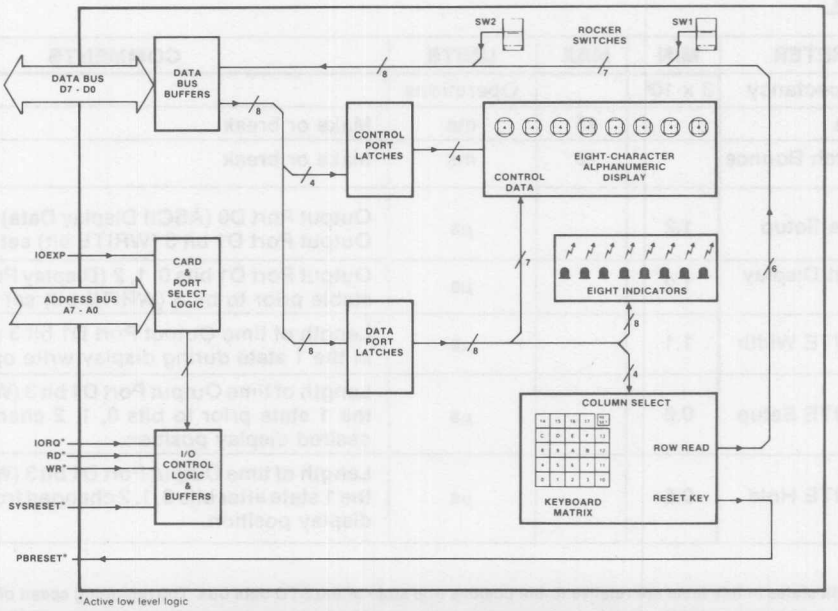
The 7303 is suitable for applications where a low cost interface is needed for system control, data entry, status display, and operator prompting. The card is also useful for system development, testing, and training applications.

The 7303 can be mounted in the first position in a card cage with an open-end panel, on a card extender such as the 7901, or panel mounted on up to ⅛-in. (3.18 mm) panel stock.



FEATURES

- **8-position Alphanumeric Display with ASCII Input**
- **24 Programmable Keys Plus Reset**
- **Repairable Keyboard and Replaceable Key Labels**
- **8-bit Binary LED Display**
- **2 Rocker Switches**
- **Simple Program Control of Displays and Keys**
- **On-card I/O Ports for Processor Control**
- **Single +5V Operation**
- **Universal Processor Compatibility—Z80, 8085, 6800, and others**



*Active low level logic

7303 KEYBOARD/DISPLAY CARD

FUNCTIONAL

Card Address Mapping

The 7303 is selected by a decoded combination of address lines A1-A7. The user chooses the card address combination by connecting one jumper wire each from SX and SY to pad matrices adjacent to decoders U3 and U4. The 7303 is shipped with hex port addresses D0 and D1 selected by jumper wires.

Port Addresses

Address line A0 selects one of two sequential port addresses on the 7303. One input port and one output port resides at the hex D0 address, and one-half output port (bits D0-D3) resides at the hex D1 address. The RD* and WR* lines control the input gating or output latching.

Alphanumeric Display

This display consists of eight, 16-segment display digit positions. Each position has an internal latch that accepts one of 64 ASCII coded characters. The latch eliminates the need for display refreshing and allows each display position to be changed in random order without disturbing the other positions. Each position can display 64 characters including the space character (all segments off), plus a cursor (all segments on). The cursor can be displayed without altering the position's ASCII character memory. Output Port D0 (ASCII data and cursor control) and Output Port D1 (display position select and write control) drive the alphanumeric display. Manipulation of these output ports controls the display's operation.

Keyboard

The 25-key keyboard includes a reset key, which grounds the 7303's PBRESET* Output when depressed, and 24 program-definable keys wired in a 4-in. x 6-in. (102 x 152 mm) matrix. These 24 keys are sensed and decoded by the microprocessor card used to drive the 7303. The matrix columns are driven by Output Port D0 (bits 0-3) and the matrix rows are sensed by Input Port D0 (bits 0-5). As an output port bit is shifted across the columns, a key closure connects the bit to an input port line. These row and column coordinates enable the microprocessor to identify a unique key closure.

8-bit Binary LED Display

The LED display is connected to Output Port D0 and displays its data content (LED on = bit positive true). This display changes with both keyboard and alphanumeric display operations. If used to display different information, the LEDs must be refreshed after each keyboard or alphanumeric display operation.

Rocker Switches

Two rocker-type toggle switches are connected to Input Port D1 (bits 6 and 7). This input port may be read at any time to determine the position of both switches.

ELECTRICAL

PARAMETER	MIN	MAX	UNITS	COMMENTS
Key Life Expectancy	3×10^6		Operations	
Key Bounce		15	ms	Make or break
Rocker Switch Bounce		15	ms	Make or break
Display Data Setup	1.2		μs	Output Port D0 (ASCII Display Data) stable prior to Output Port D1 bit 3 (WRITE bit) set to the 1 state.
Display Digit Display Setup	1.2		μs	Output Port D1 bits 0, 1, 2 (Display Position Select) stable prior to bit 3 (WRITE bit) set to the 1 state.
Display WRITE Width	1.1		μs	Length of time Output Port D1 bit 3 (WRITE bit) is in the 1 state during display write operations.
Display WRITE Setup	0.6		μs	Length of time Output Port D1 bit 3 (WRITE bit) is in the 1 state prior to bits 0, 1, 2 changed from the desired display position.
Display WRITE Hold	0.5		μs	Length of time Output Port D1 bit 3 (WRITE bit) is in the 1 state after bits 0, 1, 2 changed from the desired display position.

NOTE

References to bit states in this table are relative to the positive true state of the STD data bus. The operating speed of the 7303's alphanumeric display may be exceeded if a fast processor card or a very short instruction sequence is used to generate the signals required. Insertion of NOP (no operation) instructions in the instruction sequence will reduce the operating speed of the program to the table values or greater.

ELECTRICAL (continued)

- Vcc = +5V ±5%
- Icc = 600mA maximum (300mA typical) with all display segments and binary LEDs on.
- Address, data, and control buses meet all STD BUS general electrical specifications, with the exception of WR*, which is 2 LSTTL input loads.

MECHANICAL

- The storage and nonoperating temperature range is limited to 0° to +55°C.
- Do not expose the 7303 keyboard to fluxes, solvents, and cleaning solutions or their fumes.
- The 7303 meets all STD BUS general mechanical specifications with the exception of component height, which is 0.95 in. (24.13 mm) maximum. As an operator interface card, access to the component side is required by the operator. This is possible in one of three ways without requiring more than one card rack slot:

  1. Insert the card in the left-most card rack socket (viewed from the card ejector end of the rack) with an open left-hand card rack end plate allowing access to the component side of the 7303.
  2. Insert a 7901 card extender in any card slot and plug the 7303 into the card extender. In this position the 7303 clears the other cards and is accessible to the operator.
  3. Mount the 7303 in panel stock of up to a ⅛-in. (3.18 mm) thickness. Four mounting holes are 1provided on the card and the display bezel is recessed approximately ⅜-in. (9.53 mm) below the keycaps and binary LEDs. This allows for beveling around the display cutout when the keys and LEDs protrude from the panel front (see diagram). Ask for Pro-Log Application Note *PLAN 131.*

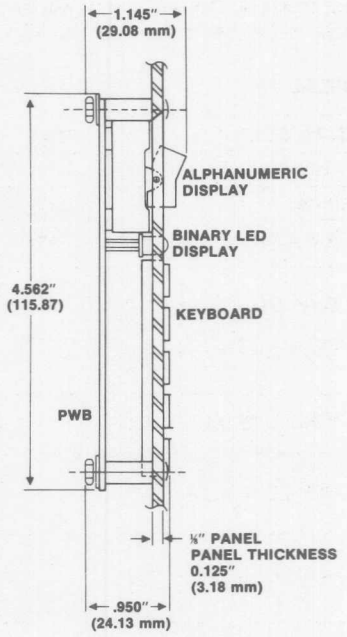
User's Manual

To obtain the user's manual for the 7303, ask for Pro-Log document #105999.

STD/7303 EDGE CONNECTOR PIN LIST							
PIN NUMBER				PIN NUMBER			
OUTPUT (LSTTL DRIVE)						OUTPUT (LSTTL DRIVE)	
INPUT (LSTTL LOADS)						INPUT (LSTTL LOADS)	
MNEMONIC							MNEMONIC
+5V	VCC		2	1		VCC	+5V
GROUND	GND		4	3		GND	GROUND
-5V			6	5			-5V
D7	1	55	8	7	55	1	D3
D6	1	55	10	9	55	1	D2
D5	1	55	12	11	55	1	D1
D4	1	55	14	13	55	1	D0
A15			16	15		1	A7
A14			18	17		1	A6
A13			20	19		1	A5
A12			22	21		1	A4
A11			24	23		1	A3
A10			26	25		1	A2
A9			28	27		1	A1
A8			30	29		1	A0
RD*	1		32	31		2	WR*
MEMRQ*			34	33		1	IORQ*
MEMEX			36	35		1	IOEXP
MCSYNC*			38	37			REFRESH*
STATUS 0*			40	39			STATUS 1*
BUSRQ*			42	41			BUSAK*
INTRQ*			44	43			INTAK*
NMIRQ*			46	45			WAITRQ*
PBRESET*		OUT	48	47		1	SYSRESET*
CNTRL*			50	49			CLOCK*
PCI	IN		52	51	OUT		PCO
AUX GND			54	53			AUX GND
AUX -V			56	55			AUX +V

*Active low level logic

Edge Connector Pins for the 7303.

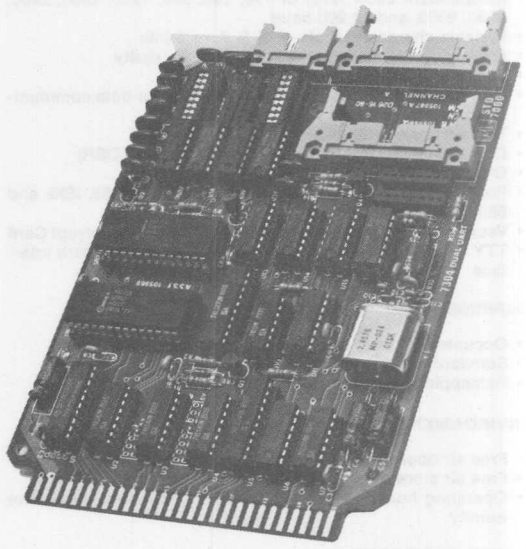


7303 Profile Mounted in User's 1/8" (3.18 mm) Panel

7000
STD BUS

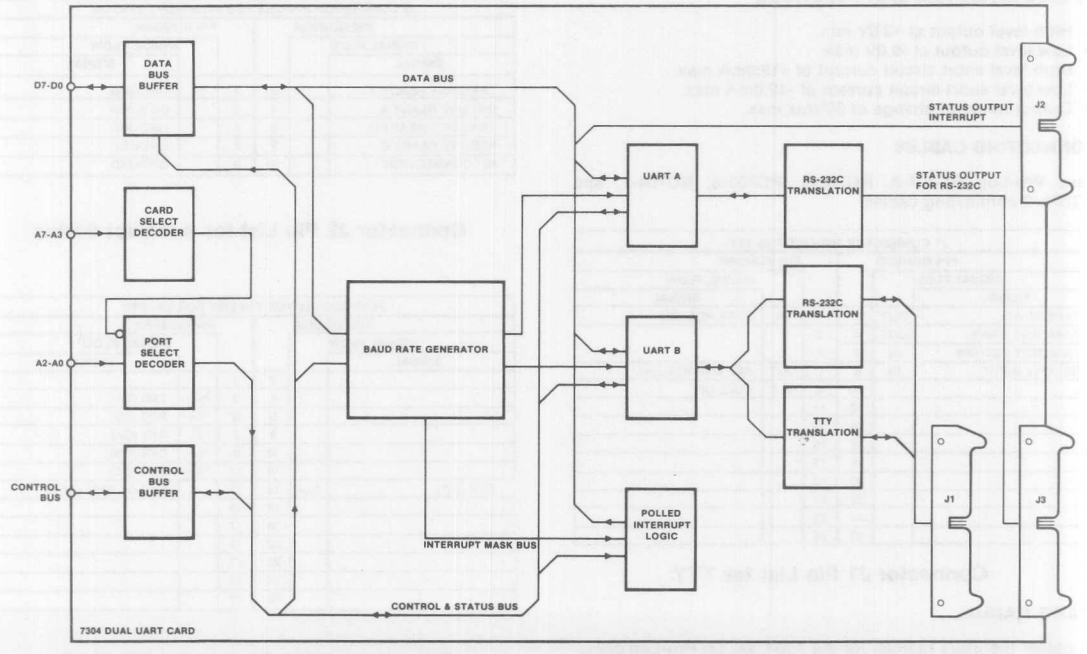
7304
DUAL UART CARD

The 7304 provides two, fully independent, RS-232C serial data communication channels on a single STD card. Asynchronous operation up to 19,200 baud is supported for full duplex DTE (Data Terminal Equipment) or DCE (Data Communications Equipment) applications. Capabilities include a TTY interface provision for one channel and polled interrupt logic for both channels.



FEATURES

- **RS-232C serial interface specification**
- **Dual, independent UARTs**
- **Independent program selectable baud rates to 19,200 baud for RS-232C**
- **Independent polled interrupt logic**
- **Connection available for 7320 priority interrupt card**
- **Selectable DTE/DCE configuration for each channel**
- **Dual 26-pin male header connectors**
- **+5V, ±12V operation**
- **Standard Pro-Log TTY interface circuit**
- **Universal processor compatability—Z80, 8085, 6800, and others**



7304 DUAL UART CARD

FUNCTIONAL CAPABILITY

- Asynchronous RS-232C operation to 19,200 baud
- Independent baud rates of 110, 150, 300, 1200, 1800, 2400, 4800, 9600, and 19,200 baud
- Variable character length of 5, 6, 7, or 8 bits
- Optional parity checking for odd or even parity
- Variable stop time of 1, 1½ or 2 stop bits
- Configuration for data terminal equipment or data communications equipment
- Transmit handshake capability (CTS, RTS)
- Equipment status handshake capability (DTR, DSR)
- Overrun detection
- Polled interrupt logic on-board for use with 8085, Z80, and 6800
- Vectored interrupt available using 7320 Priority Interrupt Card
- TTY interface for one channel using Pro-Log standard interface

MAPPING

- Occupies 8 READ/WRITE ports
- Standard mapping of E0 through E7
- Remapping allowed by changing wire jumpers

ENVIRONMENTAL SPECIFICATIONS

- Free air operating temperature from 0°C to 55°C
- Free air storage temperature from -40°C to 75°C
- Operating humidity from 5% to 95% noncondensing relative humity

POWER REQUIREMENTS

- Vcc requirement of +5 ±0.25V at 660mA max
- Aux +V requirement of +12 ±0.60V at 120mA max.
- Aux -V requirement of -12 ±0.60V at 120mA max.

RS-232C INTERFACE SPECIFICATIONS

- High level output at +9.0V min.
- Low level output at -9.0V max.
- High level short circuit current of +12.0mA max.
- Low level short circuit current of -12.0mA max.
- Output range of change of 30V/μs max.

CONNECTING CABLES

Uses Pro-Log RC701-3, RC702-3, RC703-3, RC704-1, and RC704-2 connecting cables

J1 CONNECTOR PIN LIST FOR TTY					
PIN NUMBER			PIN NUMBER		
SIGNAL FLOW				SIGNAL FLOW	
SIGNAL					SIGNAL
TAPE DRIVE	OUT	2	1	IN	TAPE RETURN
TRANSMIT DRIVE	OUT	4	3		
TRANSMIT RETURN	IN	6	5		
RECEIVE INPUT	IN	8	7	OUT	RECEIVE RETURN
		10	9	OUT	PULL-UP
		12	11		
		14	13		
		16	15		
		18	17		
		20	19		
		22	21		
		24	23		
		26	25		

Connector J1 Pin List for TTY

USER'S MANUAL

To obtain the users manual for the 7304, ask for Pro-Log document #106242.

STD 7304 EDGE CONNECTOR PIN LIST							
PIN NUMBER				PIN NUMBER			
OUTPUT (LSTTL DRIVE)						OUTPUT (LSTTL DRIVE)	
INPUT (LSTTL LOADS)						INPUT (LSTTL LOADS)	
MNEMONIC							MNEMONIC
+5 V	IN		2	1		IN	+5 V
GROUND	IN		4	3		IN	GROUND
-5V			6	5			-5V
D7	1	55	8	7	55	1	D3
D6	1	55	10	9	55	1	D2
D5	1	55	12	11	55	1	D1
D4	1	55	14	13	55	1	D0
A15			16	15		1	A7
A14			18	17		1	A6
A13			20	19		1	A5
A12			22	21		1	A4
A11			24	23		1	A3
A10			26	25		1	A2
A9			28	27		1	A1
A8			30	29		1	A0
RD*	1		32	31	1		WR*
MEMRQ*			34	33	1		IORQ*
MEMEX			36	35	1		IOEXP
MCSYNC*			38	37			REFRESH*
STATUS 0*			40	39			STATUS 1*
BUSRQ*			42	41			BUSAK*
INTRQ*		55	44	43	1		INTAK*
NMIRQ*			46	45			WAITRQ*
PBRESET*			48	47	1		SYSRESET*
CNTRL*			50	49			CLOCK*
PCI	IN		52	51		OUT	PCO
AUX GND			54	53			AUX GND
AUX -V (-12V)	IN		56	55	IN		AUX +V (+12V)

*Active low level logic

Edge Connector Pin List

J2 CONNECTOR PIN LIST FOR INTERRUPT STATUS					
PIN NUMBER			PIN NUMBER		
SIGNAL FLOW				SIGNAL FLOW	
SIGNAL					SIGNAL
TRANSMIT READY A		2	1		GROUND
RECEIVE READY A		4	3		GROUND
TRANSMIT READY B		6	5		GROUND
RECEIVE READY B		8	7		GROUND
NO CONNECTION		10	9		GROUND

Connector J2 Pin List for Interrupt Status

J1/J3 CONNECTOR PIN LIST FOR RS-232C					
PIN NUMBER			PIN NUMBER		
SIGNAL FLOW				SIGNAL FLOW	
SIGNAL					SIGNAL
		2	1		
		4	3	IN/OUT	TXD (BA)
		6	5	IN/OUT	RXD (BB)
		8	7	IN/OUT	RTS (CA)
		10	9	IN/OUT	CTS (CB)
		12	11	IN/OUT	DSR (CC)
DTR (CD)	IN/OUT	14	13		SIGNAL GND (AB)
		16	15		
		18	17		
		20	19		
		22	21		
		24	23		
		26	25		

Connector J1/J3 Pin List for RS-232C

7000
STD BUS

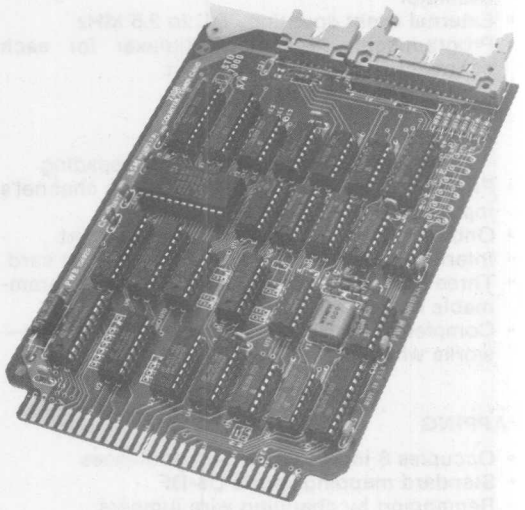
7308
COUNTER/TIMER CARD

The 7308 is a fully programmable, multichannel counter/timer card. It runs as a stand-alone peripheral after receiving setup instructions from the system processor card. An onboard interrupt and status polling system identifies completed operations.

The 7308 provides three 16-bit counter/timer channels. Also, the card provides a crystal oscillator and tapped clock divider, an 8-input multiplexer for each channel, and programmable logic states at each clock, gate, and output signal.

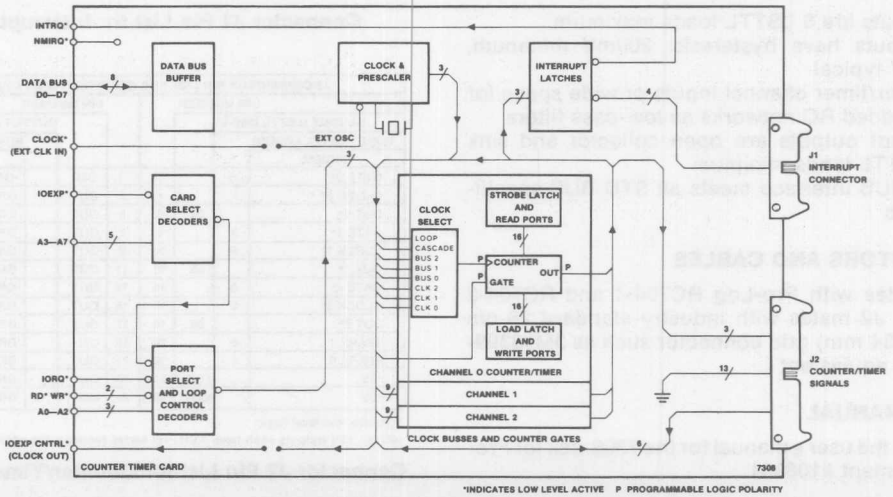
The three channels are configured independently by the program. Each is suitable for frequency/event counting from DC to 2.5 MHz, and pulse marker or square-wave generation, time interval measurements, one-shot simulation with hardware and software triggering and retriggering, and repetitive interrupt generation. A special feature allows any channel to interrupt after the n^{th} programmed event or loop iteration.

Single-channel timing over the range of 500ns to 8.3s can be programmed with 0.0015% full-scale resolution. Crystal oscillator accuracy is ±0.05% on any range.



FEATURES

- **Three independent 16-bit counter/timer channels with six operating modes each**
- **Count source multiplexer, with eight inputs for each channel (program selectable)**
- **Programmable logic polarity at user inputs and outputs**
- **No adjustments—minimizes OEM effort and field errors**
- **Onboard interrupt latches and masks for stand-alone operation**
- **STDMG-approved interrupt connector for expansion with 7320 priority interrupt card**
- **Onboard crystal oscillator for accurate programmed timing**
- **Provision for external time-reference signal input, and clock output for other STD BUS cards**
- **Universal processor compatibility: Z80, 8085A, 6800, and others**
- **Multisourced industry-standard components**
- **Single +5V operation**



*INDICATES LOW LEVEL ACTIVE P PROGRAMMABLE LOGIC POLARITY

7308 COUNTER/TIMER CARD

FUNCTIONAL CAPABILITY

- Delay, 1-shot, and rate or interrupt generator: 500ns to 8.3s with onboard 0.05% crystal oscillator
- External event counting: DC to 2.5 MHz
- Programmable 8-input multiplexer for each channel to allow counting from:
  - 3 on-card time bases
  - 3 external inputs
  - 1 program loop control, or
  - 1 adjacent channel output for cascading
- Programmable logic polarity for each channel's input and output signals
- Onboard interrupt masks and polling port
- Interface connector for vectored interrupt card
- Three fully independent channels with programmable cascading
- Completely universal processor operation—works with Z80, 8085, 6800, and others

MAPPING

- Occupies 8 input/output port addresses
- Standard mapping: ports D8-DF
- Remapping by changing wire jumpers

ENVIRONMENTAL SPECIFICATIONS

- Free-air operating temperature from 0° to 55°C
- Free-air storage temperature from -40° to +70°C
- Operating humidity from 5 to 95% noncondensing relative humidity

POWER REQUIREMENTS

- Vcc = +5V ± 0.25V at 700mA maximum, 425mA typical

INTERFACE SPECIFICATIONS

- All inputs are 5 LSTTL loads maximum
- All inputs have hysteresis: 200mV minimum, 400mV typical
- Counter/timer channel inputs provide space for user-added RC networks as low-pass filters
- Interrupt outputs are open collector and sink 10 LSTTL loads minimum
- STD BUS interface meets all STD BUS specifications

CONNECTORS AND CABLES

• J1 mates with Pro-Log RC704-1 and RC704-2 cables • J2 mates with industry standard 26-pin 0.1-in. (2.54 mm) grid connector such as 3M#3399-6026-1 or equivalent

USER'S MANUAL

To obtain the user's manual for the 7308, ask for Pro-Log document #106931.

STD/7308 EDGE CONNECTOR PIN LIST							
PIN NUMBER				PIN NUMBER			
OUTPUT (LSTTL DRIVE)						OUTPUT (LSTTL DRIVE)	
INPUT (LSTTL LOADS)						INPUT (LSTTL LOADS)	
MNEMONIC						MNEMONIC	
+5V	IN		2	1		IN	+5V
GROUND	IN		4	3		IN	GROUND
-5V			6	5			-5V
D7	1	55	8	7	55	1	D3
D6	1	55	10	9	55	1	D2
D5	1	55	12	11	55	1	D1
D4	1	55	14	13	55	1	D0
A15			16	15		1	A7
A14			18	17		1	A6
A13			20	19		1	A5
A12			22	21		1	A4
A11			24	23		1	A3
A10			26	25		1	A2
A9			28	27		1	A1
A8			30	29		1	A0
RD*	1		32	31		1	WR*
MEMRQ*			34	33		1	IORQ*
MEMEX			36	35		1	IOEXP
MCSYNC*			38	37			REFRESH*
STATUS 0*			40	39			STATUS 1*
BUSRQ*			42	41			BUSAK*
INTRQ*		[a]	44	43			INTAK*
NMIRQ*			46	45			WAITRQ*
PBRESET*			48	47			SYSRESET*
CNTRL*			50	49			CLOCK*
PCI	IN		52	51		OUT	PCO
AUX GND			54	53			AUX GND
AUX -V			56	55			AUX +V

* Active low-level logic [a] Open-collector driver

Edge Connector Pin List

J1 CONNECTOR PIN LIST FOR INTERRUPT STATUS						
PIN NUMBER			PIN NUMBER			
OUTPUT (LSTTL DRIVE)					OUTPUT (LSTTL DRIVE)	
INPUT (LSTTL LOADS)					INPUT (LSTTL LOADS)	
SIGNAL					SIGNAL	
HELP 0*		[a] 10	2	1	OUT	GROUND
HELP 1*		[a] 10	4	3	OUT	GROUND
HELP 2*		[a] 10	6	5	OUT	GROUND
GROUP*		[a] 10	8	7	OUT	GROUND
TEST		0	10	9	OUT	GROUND

* Active low-level logic [a] Open-collector driver

Connector J1 Pin List for Interrupt Status

J2 CONNECTOR PIN LIST FOR COUNTER/TIMER CHANNELS						
PIN NUMBER			PIN NUMBER			
OUTPUT (LSTTL DRIVE)					OUTPUT (LSTTL DRIVE)	
INPUT (LSTTL LOADS)					INPUT (LSTTL LOADS)	
SIGNAL					SIGNAL	
GATE 0*	5		2	1	OUT	GROUND
CLOCK 0*	5		4	3	OUT	GROUND
OUT 0*		55	6	5	OUT	GROUND
GATE 1*	5		8	7	OUT	GROUND
CLOCK 1*	5		10	9	OUT	GROUND
OUT 1*		55	12	11	OUT	GROUND
GATE 2*	5		14	13	OUT	GROUND
CLOCK 2*	5		16	15	OUT	GROUND
OUT 2*		55	18	17	OUT	GROUND
SPARE 1	5		20	19	OUT	GROUND
SPARE 0	5		22	21	OUT	GROUND
+5V		OUT	24	23	OUT	GROUND
+5V		OUT	26	25	OUT	GROUND

* Active low-level logic

NOTE: +5V outputs each have 1.0Ω, ¼W series resistors for connector protection.

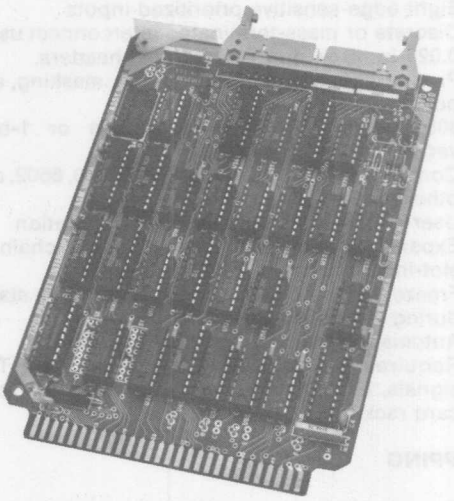
Connector J2 Pin List for Counter/Timer Channels

7000
STD BUS

7320
PRIORITY INTERRUPT CARD

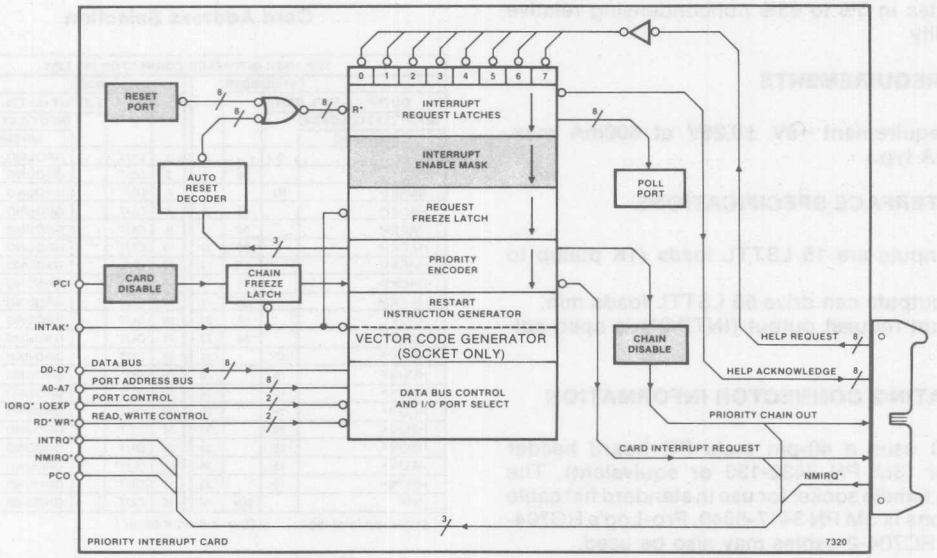
The 7320 is a universal, 8-input, Priority Interrupt Controller for TTL-compatible interrupt requests originating in the same card rack. The card accepts interrupt requests from other cards, prioritizes them, and generates a single interrupt request to the system microprocessor card. Polled interrupts, 8080-family RESTART instructions, and high-speed single-byte vectored interrupts are all supported with automatic resetting of the interrupt request latches to minimize program service time.

A card level priority system allows 7320s to be cascaded at the user interface connector or across the STD BUS priority chain. Hysteresis buffers, edge-sensitive latches, and interrupt system freeze circuitry are combined to provide error-free operation.



FEATURES

- **Eight, Prioritized, Edge-sensitive Inputs**
- **Program Control of Interrupt Polling, Masking, and Clearing**
- **Programmable Priority Chain Participation**
- **Universal:**
  1-byte Vector PROM Socket for Z80 (Mode 2)
  RESTART generator for 8085 and Z80 (Mode 0)
  Polled Mode for 6800 Family and Others
- **Automatic Latch Clearing for Minimized Service Routine**
- **Universal Processor Compatibility—Z80, 8085, 6800, and others**



☐ Shading indicates programmable function.

7320 PRIORITY INTERRUPT CARD

FUNCTIONAL

- Eight edge-sensitive prioritized inputs
- Discrete or mass-terminated interconnect using 0.025-in. (0.64 mm) square post headers.
- Program control of input latching, masking, and polling
- 8080-family RESTART instruction or 1-byte vector generation
- Compatible with Z80, 8085, 8080, 6800, 6502, and other processor cards
- User-supplied PROM for vector generation
- Expandable via motherboard priority chain or slot-independent card front daisy chain
- Freeze latches prevent change in system status during interrupt acknowledge (INTAK*)
- Automatic request latch reset by INTAK*
- Requires signal conditioning for non-TTL signals, or signals generated outside the local card rack

MAPPING

- Occupies 4 READ/WRITE I/O port addresses
- Standard mapping hexadecimal CC through CF
- Remapping allowed by changing wire jumpers

ENVIRONMENTAL SPECIFICATIONS

- Free air operating temperature ranges from 0°C to +55°C ambient
- Free air storage temperature from -40°C to +75°C
- Operates in 5% to 95% noncondensing relative humidity

POWER REQUIREMENTS

- Vcc requirement +5V ±0.25V at 800mA max. (460mA typ.)

USER INTERFACE SPECIFICATIONS

- User inputs are 15 LSTTL loads (1K pullup to +5V)
- User outputs can drive 55 LSTTL loads min.
- Interrupt request output (INTRQ*) is open collector

USER MATING CONNECTOR INFORMATION

The 7320 uses a 40-pin male PC board header connector (3M PN 3432-130 or equivalent). The matching female socket for use in standard flat cable applications is 3M PN 3417-6040. Pro-Log's RC704-1 and/or RC704-2 cables may also be used.

USER'S MANUAL

To obtain the user's manual for the 7320, ask for Pro-Log document #106178.

STD/7320 EDGE CONNECTOR PIN LIST							
PIN NUMBER				PIN NUMBER			
OUTPUT (LSTTL DRIVE)						OUTPUT (LSTTL DRIVE)	
INPUT (LSTTL LOADS)							INPUT (LSTTL LOADS)
MNEMONIC							MNEMONIC
+5 V	VCC		2	1		VCC	+5 V
GROUND	GND		4	3		GND	GROUND
-5V			6	5			-5V
D7	1	55	8	7	55	1	D3
D6	1	55	10	9	55	1	D2
D5	1	55	12	11	55	1	D1
D4	1	55	14	13	55	1	D0
A15			16	15		1	A7
A14			18	17		1	A6
A13			20	19		1	A5
A12			22	21		1	A4
A11			24	23		1	A3
A10			26	25		1	A2
A9			28	27		1	A1
A8			30	29		1	A0
RD*	1		32	31		1	WR*
MEMRQ*			34	33		1	IORQ*
MEMEX			36	35		1	IOEXP
MCSYNC*			38	37			REFRESH*
STATUS 0*			40	39			STATUS 1*
BUSRQ*			42	41			BUSAK*
INTRQ*		20#	44	43		1	INTAK*
NMIRQ*		OUT	46	45			WAITRQ*
PBRESET*			48	47		1	SYSRESET*
CNTRL*			50	49			CLOCK*
PCI	5		52	51	55		PCO
AUX GND			54	53			AUX GND
AUX -V (-12V)			56	55			AUX +V (-12V)

* Active low-level logic # Open-collector driver

Card Address Selection

7320 USER INTERFACE CONNECTOR PIN LIST							
PIN NUMBER				PIN NUMBER			
OUTPUT (LSTTL DRIVE)						OUTPUT (LSTTL DRIVE)	
INPUT (LSTTL LOADS)							INPUT (LSTTL LOADS)
MNEMONIC							MNEMONIC
INH*	5		2	1	OUT		GROUND
PCO		55	4	3	OUT		GROUND
NMIRQ*	IN		6	5	OUT		GROUND
HACK7*		55	8	7	OUT		GROUND
HACK6*		55	10	9	OUT		GROUND
HACK5*		55	12	11	OUT		GROUND
HACK4*		55	14	13	OUT		GROUND
HACK3*		55	16	15	OUT		GROUND
HACK2*		55	18	17	OUT		GROUND
HACK1		55	20	19	OUT		GROUND
HACK0*		55	22	21	OUT		GROUND
HELP7*	15		24	23	OUT		GROUND
HELP6*	15		26	25	OUT		GROUND
HELP5*	15		28	27	OUT		GROUND
HELP4*	15		30	29	OUT		GROUND
HELP3*	15		32	31	OUT		GROUND
HELP2*	15		34	33	OUT		GROUND
HELP1*	15		36	35	OUT		GROUND
HELP0*	15		38	37	OUT		GROUND
INT*		20#	40	39	OUT		GROUND

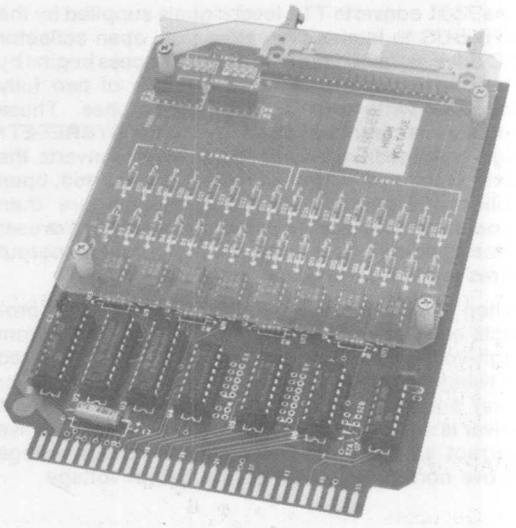
* Active low-level logic # Open-collector driver

User Interface Connector Pin List

7000 STD BUS

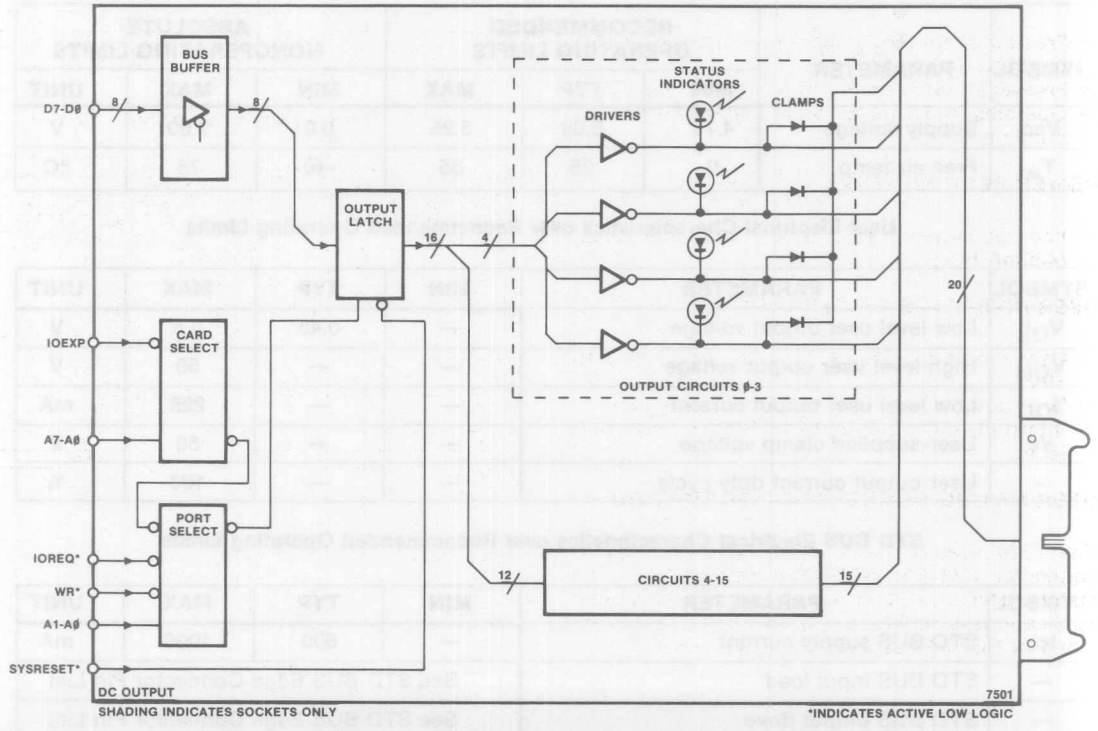
7501 MEDIUM POWER DC DRIVER CARD

The 7501 provides sixteen independent DC output circuits for the 7000 Series STD BUS. Each open collector output circuit is capable of sinking up to +225mA of current in the on-state and can withstand a +50V output level in the off-state. Diode clamping is included to limit the output voltage when driving inductive loads. Separate user-supplied clamp voltage inputs are provided for each group of four outputs. Sixteen LEDs provide a visual indication of the state of the outputs.



FEATURES

- **16 Independent DC Output Circuits**
- **+225mA Current Sink Rate**
- **+50V Output Rating**
- **Diode Clamp for Driving Inductive Loads**
- **Ground Return for each Output Circuit**
- **LED Indicator for each Output Circuit**
- **Standard 40-pin Flat Cable Connector**
- **Clear Plastic Safety Shields**
- **Universal Processor Compatibility—Z80, 8085, 6800, and others.**



7501 MEDIUM POWER DC DRIVER CARD

FUNCTIONAL

Operation

The 7501 converts TTL level signals supplied by the STD BUS to latched, negative true, open collector DC drive signals. This conversion process begins by strobing eight bits of data into one of two fully decoded write-only output port latches. These latches are cleared at power-on by the SYSRESET* signal. A medium power logic driver converts the sixteen latched output signals to an inverted, open collector signal. The driver's outputs are then brought to a 40-pin flat cable connector at the user interface card edge. Alternating ground and output wires minimize crosstalk on the flat cable.

When driving inductive loads, a diode clamp protects each medium power logic driver output from high-voltage breakdown. This diode is connected between the user-supplied clamp voltage (+50V or less) and the output signal line. When the logic driver is switched off (no current sink), the inductive current surge raises the collector output voltage above normal levels. When the output voltage exceeds the clamp voltage, the clamp diode will limit the collector voltage to approximately the clamp voltage. A separate clamp voltage input is provided for each group of four outputs (16 outputs, 4 groups) at the user interface connector. The clamp voltage must be greater than or equal to the off-state output voltage for each output, but less than +50V. All output signals are monitored for the low (active) state by LEDs. A diode protects each LED from reverse voltage breakdown.

Mapping

The 7501 consists of two 8-bit output ports that may be placed anywhere in the I/O address space of 00-FF. These ports occupy two consecutive address locations. The 7501 is shipped with hexadecimal port address 40 (port 0 address) and port address 41 (port 1 address). These port addresses are selected by jumper wires. For additional information, see *User's Manual.*

ELECTRICAL

7501 Medium Power DC Output Card Electrical Specifications

SYMBOL	PARAMETER	RECOMMENDED OPERATING LIMITS			ABSOLUTE NONOPERATING LIMITS		
		MIN	TYP	MAX	MIN	MAX	UNIT
Vcc	Supply voltage	4.75	5.00	5.25	0.0	7.00	V
T_A	Free air temp.	0	25	55	-40	75	°C

User Electrical Characteristics over Recommended Operating Limits

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{OL}	Low level user output voltage	—	0.45	0.8	V
V_{OH}	High level user output voltage	—	—	50	V
I_{OL}	Low level user output current	—	—	225	mA
Vc	User-supplied clamp voltage	—	—	50	V
-	User output current duty cycle	—	—	100	%

STD BUS Electrical Characteristics over Recommended Operating Limits

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
Icc	STD BUS supply current	—	600	1000	mA
—	STD BUS input load	See STD BUS Edge Connector Pin List			
—	STD BUS output drive	See STD BUS Edge Connector Pin List			

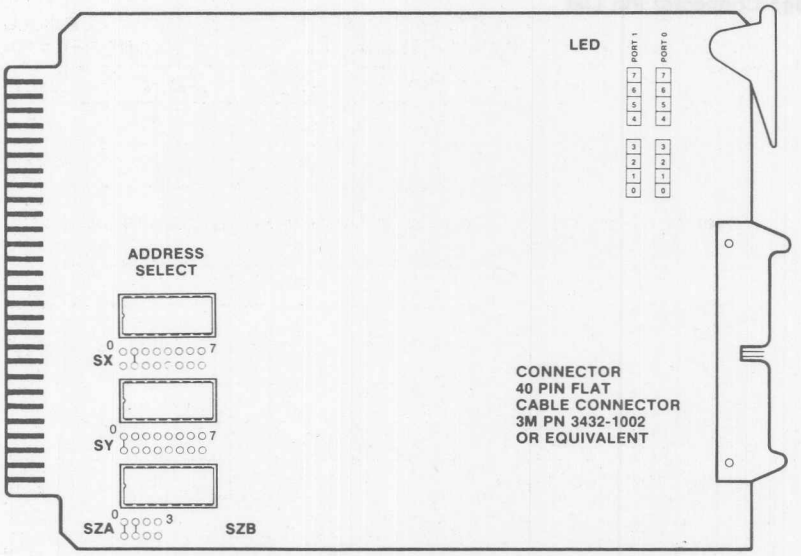
Switching Characteristics over Recommended Operating Limits

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
T_F	(Inactive-active)	—	200	240	ns
T_R	(Active-inactive)	—	200	240	ns

MECHANICAL

- Refer to the Card Address Selection diagram for component placement information.
- When placed in a Series 7000 STD BUS card rack, the 7501 requires clearances of 0.150 in. (3.81mm) on the circuit side and 0.600 in. (15.24mm) on the component side of the printed circuit board.

User Mating Connector Information
The 7501 uses a 40-pin male PC board header connector (3M PN 3432-130 or equivalent). The matching female socket for use in standard flat cable applications is 3M PN 3417-6040. RC704-1 and 704-2 cables are also compatible.



Card Address Selection

7501 MEDIUM POWER DC DRIVER CARD

STD/7501 EDGE CONNECTOR PIN LIST							
PIN NUMBER				PIN NUMBER			
OUTPUT (LSTTL DRIVE)						OUTPUT (LSTTL DRIVE)	
INPUT (LSTTL LOADS)						INPUT (LSTTL LOADS)	
MNEMONIC							MNEMONIC
+5 V	VCC		2	1		VCC	+5 V
GROUND	GND		4	3		GND	GROUND
-5V			6	5			-5V
D7	1		8	7		1	D3
D6	1		10	9		1	D2
D5	1		12	11		1	D1
D4	1		14	13		1	D0
A15			16	15		1	A7
A14			18	17		1	A6
A13			20	19		1	A5
A12			22	21		1	A4
A11			24	23		1	A3
A10			26	25		1	A2
A9			28	27		1	A1
A8			30	29		1	A0
RD*	1		32	31		1	WR*
MEMRQ*			34	33		1	IORQ*
MEMEX			36	35		1	IOEXP
MCSYNC*			38	37			REFRESH*
STATUS 0*			40	39			STATUS 1*
BUSRQ*			42	41			BUSAK*
INTRQ*			44	43			INTAK*
NMIRQ*			46	45			WAITRQ*
PBRESET*			48	47		1	SYSRESET*
CNTRL*			50	49			CLOCK*
PCI	IN		52	51	OUT		PCO
AUX GND			54	53			AUX GND
AUX -V			56	55			AUX +V

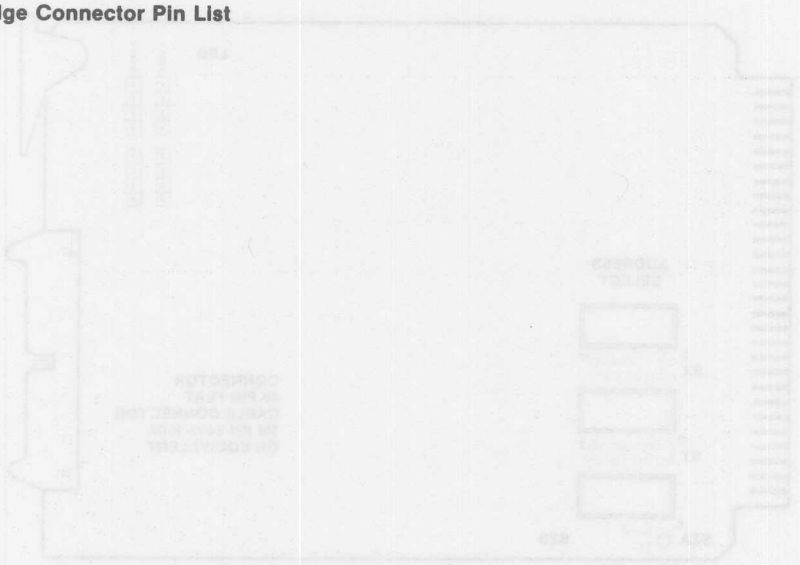
*Active low level logic

Edge Connector Pin List

STD/7501 USER CONNECTOR PIN LIST			
PIN NUMBER		PIN NUMBER	
MNEMONIC			MNEMONIC
GROUND	2	1	CLAMP 0-3
GROUND	4	3	OUTPUT 0*
GROUND	6	5	OUTPUT 1*
GROUND	8	7	OUTPUT 2*
GROUND	10	9	OUTPUT 3*
GROUND	12	11	OUTPUT 4-7
GROUND	14	13	OUTPUT 4*
GROUND	16	15	OUTPUT 5*
GROUND	18	17	OUTPUT 6*
GROUND	20	19	OUTPUT 7*
GROUND	22	21	OUTPUT 8-11
GROUND	24	23	OUTPUT 8*
GROUND	26	25	OUTPUT 9*
GROUND	28	27	OUTPUT 10*
GROUND	30	29	OUTPUT 11*
GROUND	32	31	OUTPUT 12-15
GROUND	34	33	OUTPUT 12*
GROUND	36	35	OUTPUT 13*
GROUND	38	37	OUTPUT 14*
GROUND	40	39	OUTPUT 15*

*Active low level logic

User Connector Pin List



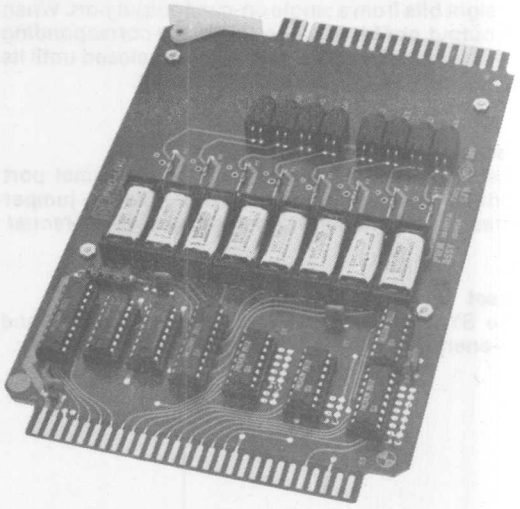
USER'S MANUAL

To obtain the user's manual for the 7501, ask for Pro-Log document #106691.

7000
STD BUS

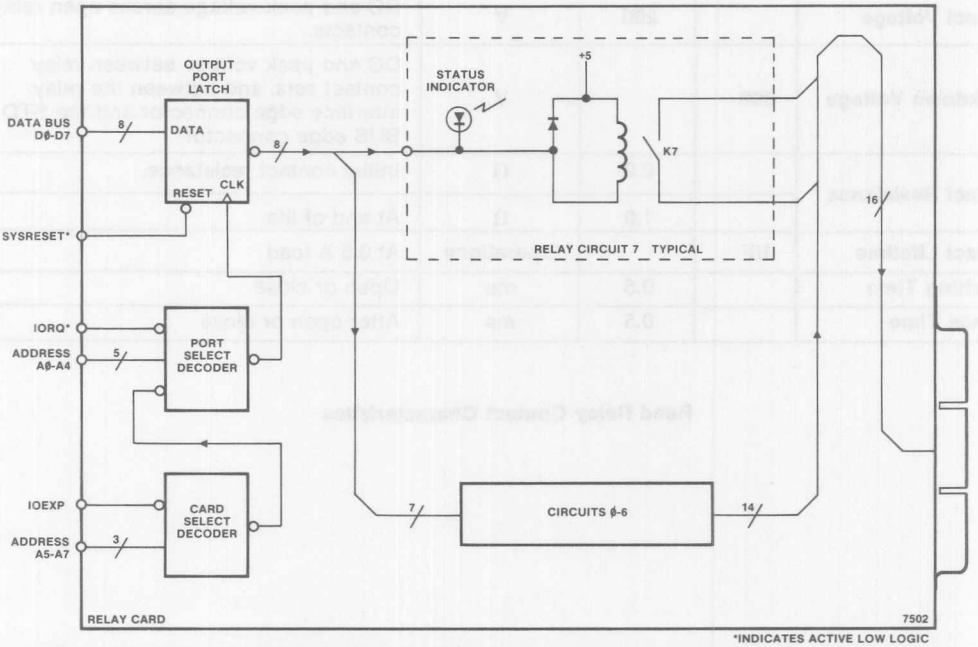
7502
SPST RELAY OUTPUT CARD

The 7502 consists of eight independent SPST dry reed relays controlled by a fully decoded, latched 8-bit output port. Each 7502 allows the processor direct control of eight additional reed relay switches.



FEATURES

- **Eight Independent SPST Dry Reed Relays**
- **On-card LED Display of Relay Driver Status**
- **User-selected Port Address**
- **Keyed Front-edge Connector for Relay Outputs**
- **Single +5V Operation**
- **Universal Processor Compatability—Z80, 8085, 6800, and others**



*INDICATES ACTIVE LOW LOGIC

7502 SPST RELAY OUTPUT CARD

FUNCTIONAL

The 7502's eight relays are switched independently by eight bits from a single on-card output port. When an output por bit is latched high, the corresponding reed relay closes. The relay remains closed until its output port bit is latched low or reset.

Card Address Mapping

The 7502 card is shipped with hexadecimal port address 40. This port address is selected by jumper wires. For additional information, see *User's Manual.*

Reset

The SYSRESET* input clears the output port and de-energizes all eight reed relays simultaneously.

ELECTRICAL

- +5V ±5%
- ICC = 400mA Maximum (300mA typical), all relays energized
- Address, data, and control buses meet all STD BUS general electrical specifications
- Pads are provided at each relay contact set for user-added RC suppression networds

PARAMETER	MIN	MAX	UNIT	COMMENT
Contact Current		0.5	A	Combined DC and peak transient currents during contact opening or
Contact Voltage		200	V	DC and peak voltage across open relay contacts.
Breakdown Voltage	300		V	DC and peak voltage between relay contact sets, and between the relay interface edge connector and the STD BUS edge connector.
Contact Resistance		0.2	Ω	Initial contact resistance.
		1.0	Ω	At end of life
Contact Lifetime	10^7		Operations	At 0.5 A load
Switching Time		0.5	ms	Open or close
Bounce Time		0.5	ms	After open or close

Reed Relay Contact Characteristics

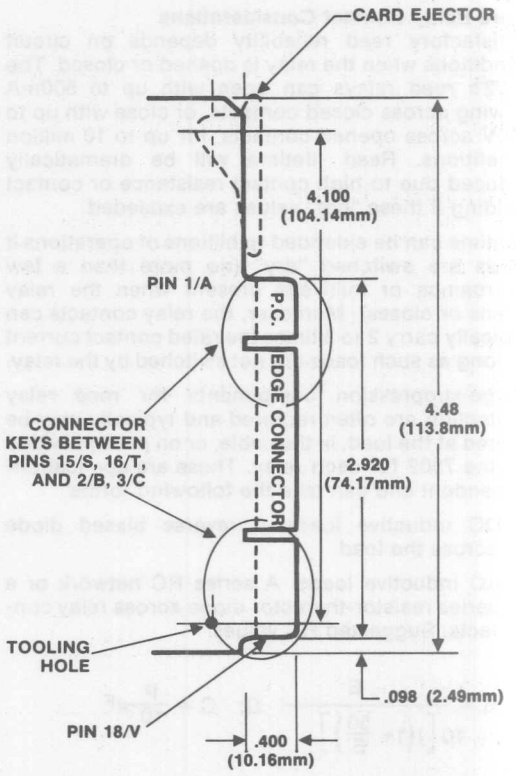
MECHANICAL

Meets all STD BUS general mechanical specifications with the following exceptions:

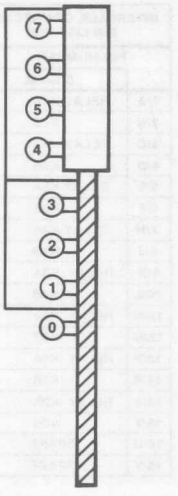
1. The I/O interface connector is a 36-pin (dual 18-pin) edge connector. Overall card length is extended to 6.90 ±0.025 in. (175.26 ±0.635mm). Edge connector height is 2.930 ±0.005 in. (74.42 ±0.305mm). Contact fingers are on 0.156 in. (3.962mm) centers. Opposing fingers are shorted, yielding 18 isolated contacts. Two nonreversible connector keys are provided between pins 2 and 3, and 15 and 16.
2. An LED relay status display, visible from the card front, is included. Each LED is illuminated by its corresponding output port bit to indicate that the relay is energized.
3. The 7502 requires one open card slot on either side for clearance of the safety shields and interface connector (three card slots total). The back shield adds 0.15 in. (3.81mm) to the card's profile on the wiring side. Safety shields may be removed if all potentials applied to the card are not dangerous.

Interface Connector Information

See CB18 and CS18 data sheets for compatible connector information.



Front Edge Connector (Component - Side View)



LED Status Display

7502 SPST RELAY OUTPUT CARD

Reed Relay Contact Considerations

Satisfactory reed reliability depends on circuit conditions when the relay is opened or closed. The 7502's reed relays can open with up to 500mA flowing across closed contacts, or close with up to 200V across opened contacts, for up to 10 million repetitions. Reed lifetime will be dramatically reduced due to high contact resistance or contact welding if these "hot" values are exceeded.

Lifetime can be extended to billions of operations if reeds are switched "dry" (no more than a few microamps or millivolts present when the relay opens or closes). Moreover, the relay contacts can typically carry 2 to 3 times the rated contact current as long as such loads are not switched by the relay.

Surge-suppression components for reed relay protection are often required and typically may be placed at the load, in the cable, or on pads provided on the 7502 for each relay. These are application-dependent and can take the following forms:

1. DC inductive loads: A reverse biased diode across the load.
2. AC inductive loads: A series RC network or a series resistor-thyrector diode across relay contacts. Suggested RC values:

$$R = \frac{E}{10\left[I\left(1+\frac{50}{E}\right)\right]}\ \Omega;\quad C = \frac{I^2}{10}\mu F$$

   where E is the voltage across the open reed contacts immediately prior to closing (not to exceed 200V), and I is the current (in amperes) flowing through the closed contacts immediately prior to opening (not to exceed 0.5A).
3. Surge loads, including capacitive loads and incandescent lamps, can be limited to a 0.5A peak with a series resistor.

USER'S MANUAL

To obtain the user's manual for the 7502, ask for Pro-Log document #106646.

STD/7502 EDGE CONNECTOR PIN LIST							
PIN NUMBER				PIN NUMBER			
OUTPUT (LSTTL DRIVE)				OUTPUT (LSTTL DRIVE)			
INPUT (LSTTL LOADS)						INPUT (LSTTL LOADS)	
MNEMONIC							MNEMONIC
+5 V	VCC		2	1		VCC	+5 V
GROUND	GND		4	3		GND	GROUND
-5V			6	5			-5V
D7	1		8	7		1	D3
D6	1		10	9		1	D2
D5	1		12	11		1	D1
D4	1		14	13		1	D0
A15			16	15		1	A7
A14			18	17		1	A6
A13			20	19		1	A5
A12			22	21		1	A4
A11			24	23		1	A3
A10			26	25		1	A2
A9			28	27		1	A1
A8			30	29		1	A0
RD			32	31		1	WR
MEMRQ			34	33		1	IORQ
MEMEX			36	35		1	IOEXP
MCSYNC			38	37			REFRESH
STATUS 0			40	39			STATUS 1
BUSRQ			42	41			BUSAK
INTRQ			44	43			INTAK
NMIRQ			46	45			WAITRQ
PBRESET			48	47		1	SYSRESET
CNTRL			50	49			CLOCK
PCI	IN		52	51	OUT		PCO
AUX GND			54	53			AUX GND
AUX -V			56	55			AUX +V

*Active low level logic

Edge Connector Pin List

INTERFACE CONNECTOR PIN LIST 7502	
PIN NUMBER	SIGNAL
1/A	RELAY K7A
2/B	K7B
3/C	RELAY K6A
4/D	K6B
5/E	RELAY K5A
6/F	K5B
7/H	RELAY K4A
8/J	K4B
9/K	RELAY K3A
10/L	K3B
11/M	RELAY K2A
12/N	K2B
13/P	RELAY K1A
14/R	K1B
15/S	RELAY K0A
16/T	K0B
17/U	SPARE
18/V	SPARE

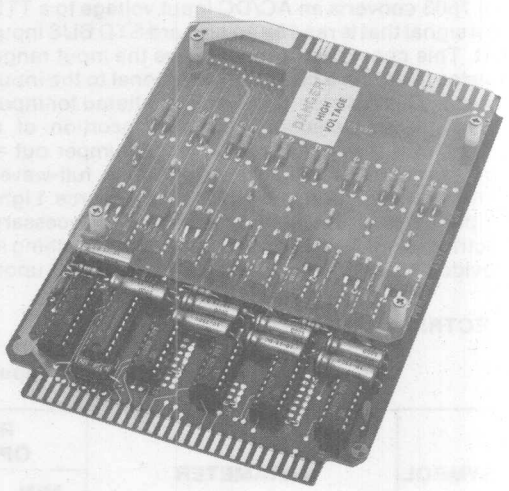
Interface Connector Pin List

7000
STD BUS

7503
OPTOISOLATED INPUT CARD

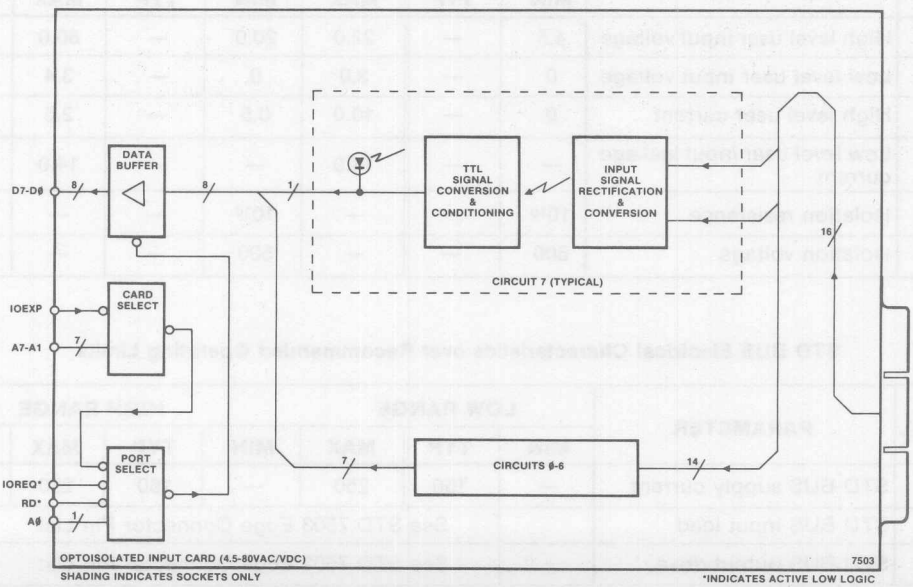
4.5-80 VAC/VDC

The 7503 provides eight independent AC/DC inputs for the Series 7000 STD BUS. An optical coupling circuit isolates each circuit from the STD BUS system and from each other. The 7503 offers a choice of two input ranges. Range selection is independent for each input and is selected through the installation of wire jumpers. The low range responds to input voltages between 4.5 VRMS and 22 VRMS for 5V, 6V, and 12V applications. The high range responds to input voltages of between 20 VRMS and 80 VRMS and is useful for systems using 24V, 28V, and 48V. An LED provides a visual indication of the state of each input.



FEATURES

- **500V Minimum Isolation between Inputs, and between each Input and System Ground**
- **Independent Range Selection for each Input**
- **Low Input Voltage Range from 4.5 VRMS to 22 VRMS**
- **High Input Voltage Range from 20 VRMS to 80 VRMS**
- **10.0mA RMS Maximum Input Loading**
- **Typical Turn-on Time of 11ms**
- **Typical Turn-off Time of 36ms**
- **LED Indicator for each Input Circuit**
- **DC Voltages may be applied with either Polarity**
- **User-selectable Input Port Address**
- **Keyed Interface Connector**
- **Clear Plastic Safety Shield**
- **Single +5V Operation**
- **Universal Processor Compatability—Z80, 8085, 6800, and others**



7503 OPTOISOLATED INPUT CARD

FUNCTIONAL

Operation

The 7503 converts an AC/DC input voltage to a TTL level signal that is read by an on-card STD BUS input port. This conversion process uses the input range resistor to obtain a current proportional to the input voltage. This resistor value may be altered for input voltage range selection with the insertion of a jumper wire (jumper in = low range, jumper out = high range). This input current is then full-wave-rectified and applied to an LED photo source. Light coupling to a photodetector provides the necessary electrical signal isolation. Analog pulse stretching is provided to assure a constant output signal upon application of a 50Hz or higher frequency input signal. The analog signal is converted to a TTL level signal, which is monitored with both an LED indicator and the STD BUS input port.

Mapping

The 7503 consists of a single, 8-bit input port that may be placed anywhere in the I/O address space of 00-FF. The 7503 is shipped with hexadecimal port address 40. For additional information, see *User's Manual.*

ELECTRICAL

7503 Optoisolated Input Card Electrical Specifications

SYMBOL	PARAMETER	RECOMMENDED OPERATING LIMITS			ABSOLUTE NONOPERATING LIMITS		
		MIN	TYP	MAX	MIN	MAX	UNIT
Vcc	Supply voltage	4.75	5.00	5.25	0.0	7.00	V
T_A	Free air temperature	0	25	55	-40	75	°C

User Electrical Characteristics over Recommended Operating Limits

SYMBOL	PARAMETER	LOW RANGE			HIGH RANGE			
		MIN	TYP	MAX	MIN	TYP	MAX	UNIT
V_{IH}	High level user input voltage	4.5	—	22.0	20.0	—	80.0	VRMS
V_{IL}	Low level user input voltage	0	—	3.0	0	—	3.4	VRMS
I_{IH}	High level user current	0	—	10.0	0.5	—	2.5	mA
I_{IL}	Low level user input leakage current	—	—	14.0	—	—	14.0	μA
R_{IO}	Isolation resistance	10^{10}	—	—	10^{10}	—	—	Ω
V_{IO}	Isolation voltage	500	—	—	500	—	—	VCD

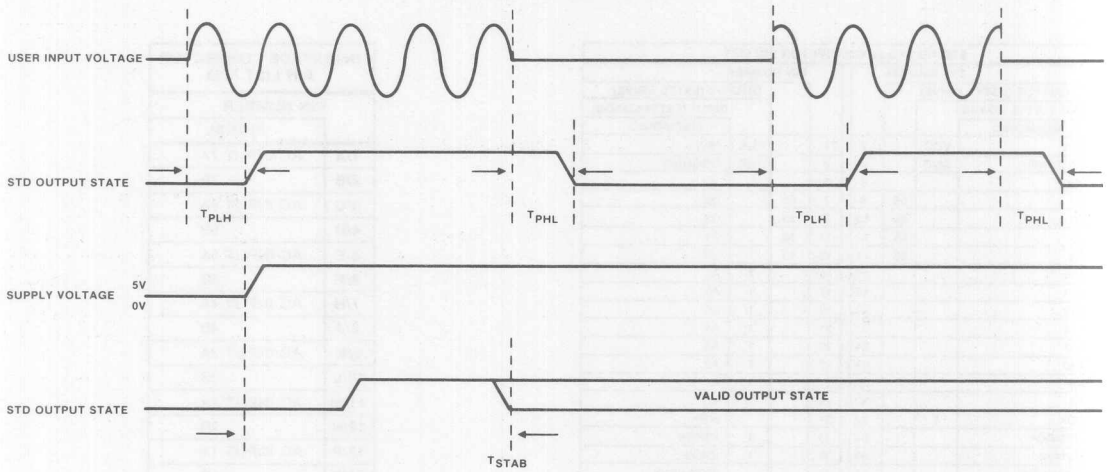
STD BUS Electrical Characteristics over Recommended Operating Limits

SYMBOL	PARAMETER	LOW RANGE			HIGH RANGE			
		MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Icc	STD BUS supply current	—	150	250	—	150	250	mA
—	STD BUS input load		See STD 7503 Edge Connector Pin List					
—	STD BUS output drive		See STD 7503 Edge Connector Pin List					

ELECTRICAL (continued)

Switching Characteristics over Recommended Operating Limits

SYMBOL	PARAMETER	FROM	TO	BOTH RANGES			COMMENTS
				MIN	TYP	MAX	
T_{PHL}	Active-Inactive	User Interface	STD Data Bus	—	36ms	200ms	See timing diagram
T_{PLH}	Inactive-Active	"	"	—	11ms	50ms	See timing diagram
T_{STAB}	Stabilize	"	"	—	50ms	250ms	See Timing diagram



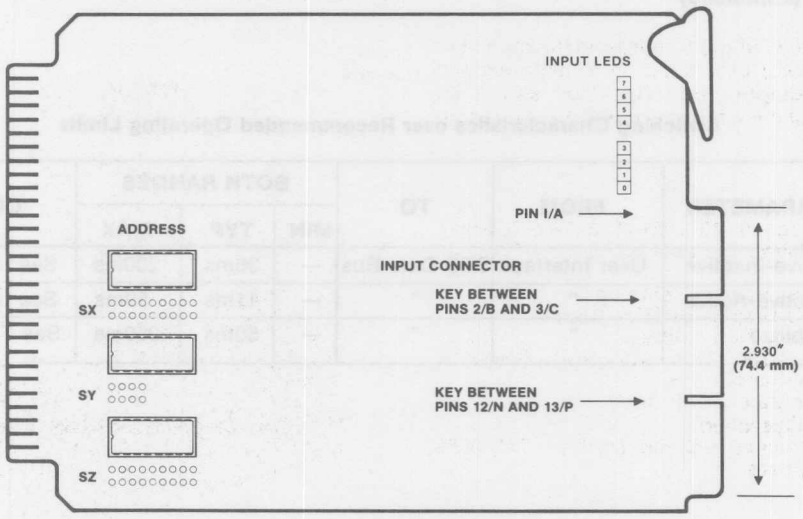
Timing Diagram

MECHANICAL

- Refer to the card address selection diagram for component placement information.
- The 7503 requires clearances of 0.150 in. (3.81mm) on the circuit side and 0.600 in. (15.24mm) on the component side of the printed circuit board when placed in a Series 7000 Card Rack.
- Clear plastic shields are provided on both sides of the assembly for protection from high voltage. Both adjacent slots must be vacant for clearance of the shields and the input connector.

Interface Connector Information
See CB18 and CS18 data sheets for compatible connector information.

7503 OPTOISOLATED INPUT CARD



Card Address Selection

STD/7503 EDGE CONNECTOR PIN LIST								
PIN NUMBER					PIN NUMBER			
OUTPUT (LSTTL DRIVE)							OUTPUT (LSTTL DRIVE)	
INPUT (LSTTL LOADS)							INPUT (LSTTL LOADS)	
MNEMONIC								MNEMONIC
+5 V	VCC		2	1		VCC	+5 V
GROUND	GND		4	3		GND	GROUND
-5V			6	5			-5V
D7		55	8	7	55		D3
D6		55	10	9	55		D2
D5		55	12	11	55		D1
D4		55	14	13	55		D0
A15			16	15		1	A7
A14			18	17		1	A6
A13			20	19		1	A5
A12			22	21		1	A4
A11			24	23		1	A3
A10			26	25		1	A2
A9			28	27		1	A1
A8			30	29		1	A0
RD*	1		32	31			WR*
MEMRQ*			34	33		1	IORQ*
MEMEX			36	35		1	IOEXP
MCSYNC*			38	37			REFRESH*
STATUS 0*			40	39			STATUS 1*
BUSRQ*			42	41			BUSAK*
INTRQ*			44	43			INTAK*
NMIRQ*			46	45			WAITRQ*
PBRESET*			48	47			SYSRESET*
CNTRL*			50	49			CLOCK*
PCI	IN		52	51	OUT		PCO
AUX GND			54	53			AUX GND
AUX -V			56	55			AUX +V

*Active low level logic

Edge Connector Pin List

INTERFACE CONNECTOR PIN LIST 7503	
PIN NUMBER	SIGNAL
1/A	AC INPUT 7A
2/B	7B
3/C	AC INPUT 6A
4/D	6B
5/E	AC INPUT 5A
6/F	5B
7/H	AC INPUT 4A
8/J	4B
9/K	AC INPUT 3A
10/L	3B
11/M	AC INPUT 2A
12/N	2B
13/P	AC INPUT 1A
14/R	1B
15/S	AC INPUT 0A
16/T	0B
17/U	SPARE
18/V	SPARE

Interface Connector Pin List

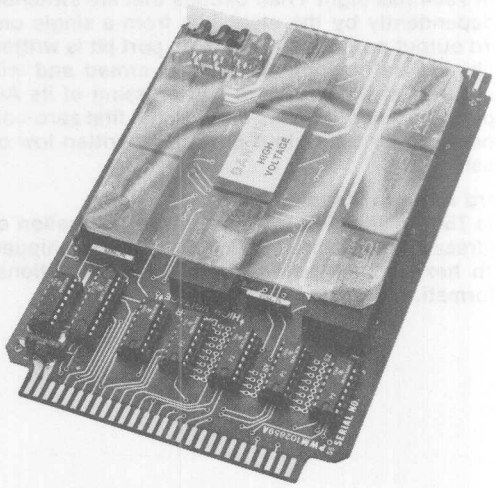
USER'S MANUAL

To obtain the user's manual for the 7503, ask for Pro-Log document #106678.

7000 STD BUS

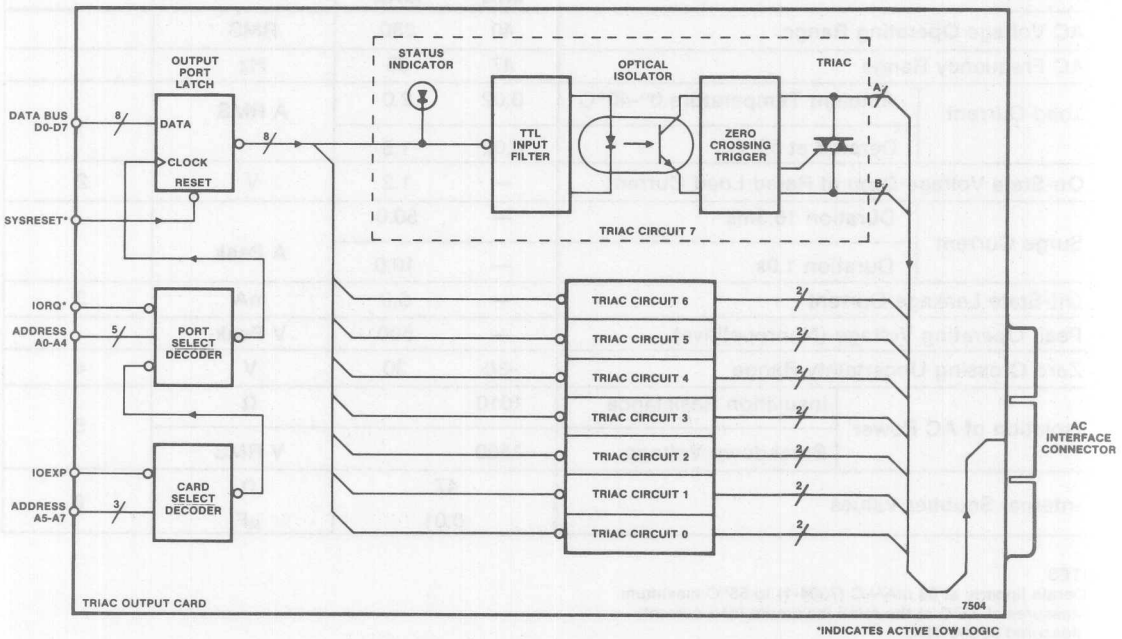
7504 TRIAC OUTPUT CARD

The 7504 consists of eight independent solid state AC relays (Triacs) controlled by a fully decoded, latched 8-bit output port. The 7504 allows the processor direct control of eight switched AC power circuits.



FEATURES

- **Eight Independent 40-280VAC 2-Amp Triacs**
- **Optical Isolation for Low Noise and 1500VAC Breakdown**
- **Zero-crossing Power Switching**
- **On-card LED Display of Triac Status**
- **User-selectable Port Address**
- **Keyed Front-edge Connector for AC Power**
- **Built-in Snubber Network**
- **Clear Plastic Safety Shields**
- **Single +5V Operation**
- **Universal Processor Compatability—Z80, 8085, 6800, and others**



7504 TRIAC OUTPUT CARD

FUNCTIONAL

Triac Switching

The 7504 has eight Triac circuits that are switched independently by the eight bits from a single on-card output port. When an output port bit is written high, the corresponding Triac is armed and will switch on at the next zero-volt crossing of its AC input. The Triac remains on until the first zero-volt crossing after the output port bit is written low or reset.

Card Address Mapping

The 7504 is selected by a decoded combination of address lines A0 through A7. The 7504 is shipped with hexadecimal port address 40. For additional information, see *User's Manual.*

Reset

The SYSRESET* input clears the output port and allows each Triac to switch off at the next zero-volt crossing of each AC input.

ELECTRICAL

- Vcc = +5V ±5%
- Icc = 500mA maximum (450mA typical)
- Address, data, and control buses meet all STD BUS general electrical specifications.
- Snubbers included. Additional snubbers may be desired at load.

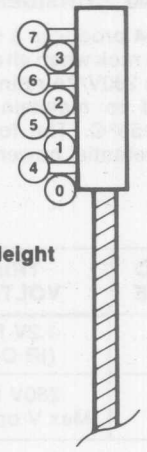
PARAMETER, Each Triac (0°C to 55°C unless noted)		7504 MIN	7504 MAX	UNITS	NOTE
AC Voltage Operating Range		40	280	RMS	
AC Frequency Range		47	63	Hz	
Load Current	Ambient Temperature 0°-40°C	0.02	2.0	A RMS	1
	Derated at 55°C	0.02	1.5		
On-State Voltage Drop at Rated Load Current		—	1.2	V	2
Surge Current	Duration 16.3ms	—	50.0	A Peak	
	Duration 1.0s	—	10.0		
Off-State Leakage Current		—	5.0	mA	3
Peak Operating Voltage (Nonrepetitive)		—	500	V Peak	
Zero Crossing Uncertainty Range		-30	30	V	4
Isolation of AC Power	Insulation Resistance	1010		Ω	5
	Breakdown Voltage	1500		V RMS	
Internal Snubber Values		47 0.01		Ω μF	6

NOTES:
1. Derate linearly at 33 mA/≐C (7504-1) to 55°C maximum.
2. Measures at 25°C at the rated maximum load current.
3. Measured at 500 VDC.
4. Describes the on/off switching characteristics of the Triac.
5. Describes the insolation between the AC power connections and the STD BUS edge connector.
6. Pads are provided for additional snubber components.

MECHANICAL

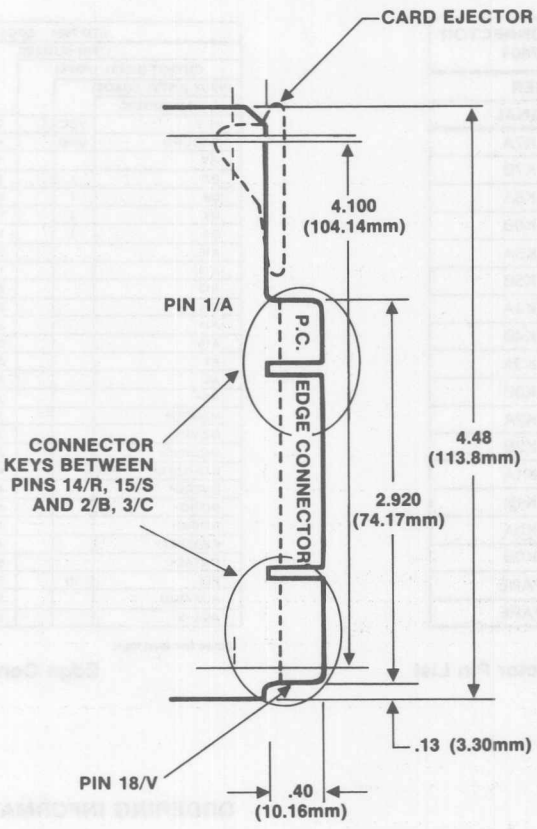
Meets all STD BUS general mechanical specifications, with the following exceptions:

1. The I/O interface connector is a 36-pin (dual 18-pin) edge connector. Overall card length is extended to 6.90 ±0.025 in. (175.26 ±0.64mm). Edge connector height is 2.920 ±0.005 in. (74.42 ±0.31mm) centers. Opposing fingers are shorted, yielding 18 isolated contacts. Two nonreversible connector keys are provided between pins 2 and 3, and 14 and 15.
2. An LED Triac status display visible from the card front is provided. Each LED is illuminated by its corresponding output port bit to indicate that the Triac is on and armed.
3. One card slot must be open on each side of the 7504 for clearance of the safety shields and interface connector (three card slots total).
4. See **Thermal Considerations.**



Maximum Component Height 0.85" (21.6mm)

LED Status Display



Front Edge Connector (Component-Side View)

7504 TRIAC OUTPUT CARD

THERMAL CONSIDERATIONS

The 7504 produces a substantial amount of heat in the card rack when all eight Triacs are operated at or near the 280V/2A rating. Forced air cooling may be required to maintain an operating temperature below +55°C. The following table illustrates the card's potential power dissipation:

The designer should determine the total "worst case" power dissipation in the application and then take precautions not to exceed the card's operating temperature. These precautions include: empty card slots adjacent to the component side of the 7504 for additional air flow, restricting the card rack's position to allow adequate air flow within the system enclosure, and forced air cooling.

TRIAC STATE	TRIAC VOLTAGE	CURRENT	POWER DISSIPATION	TOTAL OF EIGHT TRIACS	PLUS 2.625 W LOGIC POWER MAX
ON	1.2V RMS (IR Drop)	2.0A RMS (Max load)	2.4 W	19.2 W	21.825 W
OFF	280V RMS (Max V operating)	0.005A RMS (Max leakage)	1.4 W	11.2 W	13.825 W

Interface Connector Pin List

INTERFACE CONNECTOR PIN LIST 7504	
PIN NUMBER	SIGNAL
1/A	TRIAC K7A
2/B	K7B
3/C	TRIAC K6A
4/D	K6B
5/E	TRIAC K5A
6/F	K5B
7/H	TRIAC K4A
8/J	K4B
9/K	TRIAC K3A
10/L	K3B
11/M	TRIAC K2A
12/N	K2B
13/P	TRIAC K1A
14/R	K1B
15/S	TRIAC K0A
16/T	K0B
17/U	SPARE
18/V	SPARE

Interface Connector Pin List

STD 7504 EDGE CONNECTOR PIN LIST							
PIN NUMBER				PIN NUMBER			
OUTPUT (LSTTL DRIVE)						OUTPUT (LSTTL DRIVE)	
INPUT (LSTTL LOADS)						INPUT (LSTTL LOADS)	
MNEMONIC							MNEMONIC
+5 V	VCC		2	1		VCC	+5 V
GROUND	GND		4	3		GND	GROUND
-5V			6	5			-5V
D7	1		8	7		1	D3
D6	1		10	9		1	D2
D5	1		12	11		1	D1
D4	1		14	13		1	D0
A15			16	15		1	A7
A14			18	17		1	A6
A13			20	19		1	A5
A12			22	21		1	A4
A11			24	23		1	A3
A10			26	25		1	A2
A9			28	27		1	A1
A8			30	29		1	A0
RD*			32	31		1	WR*
MEMRQ*			34	33		1	IORQ*
MEMEX			36	35		1	IOEXP
MCSYNC*			38	37			REFRESH*
STATUS 0*			40	39			STATUS 1*
BUSRQ*			42	41			BUSAK*
INTRQ*			44	43		1	INTAK*
NMIRQ*			46	45			WAITRQ*
PBRESET*			48	47		1	SYSRESET*
CNTRL*			50	49			CLOCK*
PCI	IN		52	51	OUT		PCO
AUX GND			54	53			AUX GND
AUX -V			56	55			AUX +V

*Active low level logic

Edge Connector Pin List

ORDERING INFORMATION

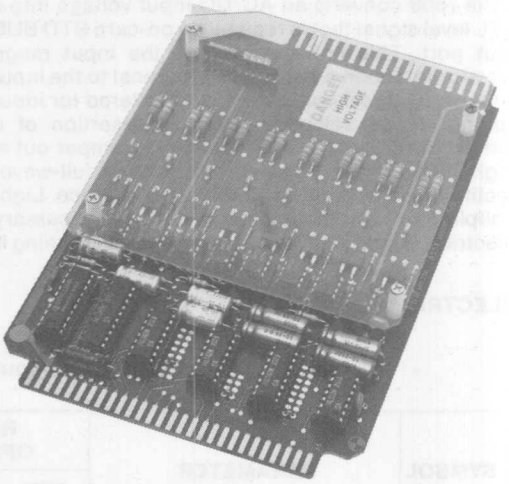
For Mating Connector Information see the CS18 or CB18 data sheet.

7000 STD BUS

7506 OPTOISOLATED INPUT CARD

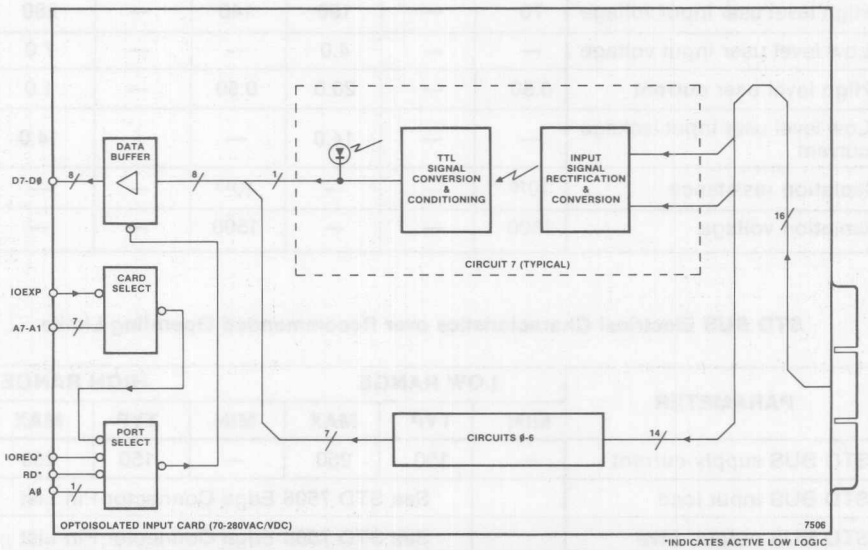
70-80 VAC/VDC

The 7506 provides eight independent AC/DC inputs for the Series 7000 STD BUS. An optical coupling circuit isolates each circuit from the STD BUS system and from each other. The 7506 offers a choice of two input ranges. Range selection is independent for each input and is selected through the installation of wire jumpers. The low range responds to input voltages of between 70 VRMS and 150 VRMS for 120V applications. The high range responds to input voltages between 140 VRMS and 280 VRMS and is useful for systems using 240V. An LED provides a visual indication of the state of each input.



FEATURES

- **500V Minimum Isolation between Inputs, and between each Input and System Ground**
- **Independent Range Selection for each Input**
- **Low Input Voltage Range from 70 VRMS to 280 VRMS**
- **High Input Voltage Range from 140 VRMS to 280 VRMS**
- **2.0mA RMS Maximum Input Loading**
- **Typical Turn-on Time of 11ms**
- **Typical Turn-off Time of 35ms**
- **LED Indicator for each Input Circuit**
- **DC Voltages may be applied with either Polarity**
- **User-selectable Input Port Address**
- **Keyed Interface Connector**
- **Clear Plastic Safety Shield**
- **Single +5V Operation**
- **Universal Procssor Compatability—Z80, 8085, 6800, and others.**



7506 OPTOISOLATED INPUT CARD

FUNCTIONAL

Operation

1The 7506 converts an AC/DC input voltage into a TTL level signal that is read by an on-card STD BUS iput port. This conversion uses the input range resistor to obtain a current proportional to the input voltage. The resistor value may be altered for input voltage range selection with the insertion of a jumper wire (jumper in = low range, jumper out = high range). This input current is then full-wave-rectified and applied to an LED photosource. Light coupling to a photodetector provides the necessary electrical signal isolation. Analog pulse stretching is provided to assure a constant output signal when a 50Hz or higher frequency AC input signal is applied. The analog signal is converted to a TTL signal that is monitored with both an LED indicator and the STD BUS input port.

Mapping

The 7506 consists of a single, 8-bit input port that may be placed anywhere in the I/O address space of OO-FF. The 7506 is shipped with hexadecimal port address 40 selected by jumper wires. For additional information, see *User's Manual.*

ELECTRICAL

7506 Optoisolated Input Card Electrical Specifications

SYMBOL	PARAMETER	RECOMMENDED OPERATING LIMITS			ABSOLUTE NONOPERATING LIMITS		
		MIN	TYP	MAX	MIN	MAX	UNIT
Vcc	Supply voltage	4.75	5.00	5.25	0.0	7.00	V
T_A	Free air temperature	0	25	55	-40	75	°C

User Electrical Characteristics over Recommended Operating Limits

SYMBOL	PARAMETER	LOW RANGE			HIGH RANGE			
		MIN	TYP	MAX	MIN	TYP	MAX	UNIT
V_{IH}	High level user input voltage	70	—	150	140	—	280	VRMS
V_{IL}	Low level user input voltage	—	—	4.0	—	—	7.0	VRMS
I_{IH}	High level user current	0.50	—	20.0	0.50	—	1.0	mA
I_{IL}	Low level user input leakage current	—	—	14.0	—	—	14.0	μA
R_{IO}	Isolation resistance	10^{10}	—	—	10^{10}	—	—	X
V_{IO}	Isolation voltage	1500	—	—	1500	—	—	VCD

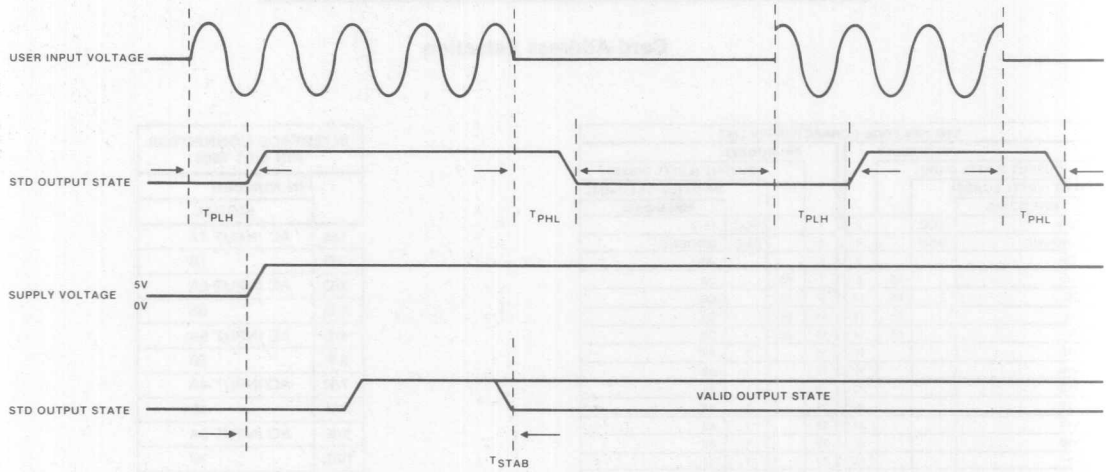
STD BUS Electrical Characteristics over Recommended Operating Limits

SYMBOL	PARAMETER	LOW RANGE			HIGH RANGE			
		MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Icc	STD BUS supply current	—	150	250	—	150	250	mA
—	STD BUS input load		See STD 7506 Edge Connector Pin List					
—	STD BUS output drive		See STD 7506 Edge Connector Pin List					

ELECTRICAL (continued)

Switching Characteristics over Recommended Operating Limits

SYMBOL	PARAMETER	FROM	TO	BOTH RANGES			COMMENTS
				MIN	TYP	MAX	
T_{PHL}	Active-Inactive	User Interface	STD Data Bus	—	36ms	200ms	See timing diagram
T_{PLH}	Inactive-Active	"	"	—	11ms	50ms	See timing diagram
T_{STAB}	Stabilize	"	"	—	50ms	250ms	See Timing diagram



Timing Diagram

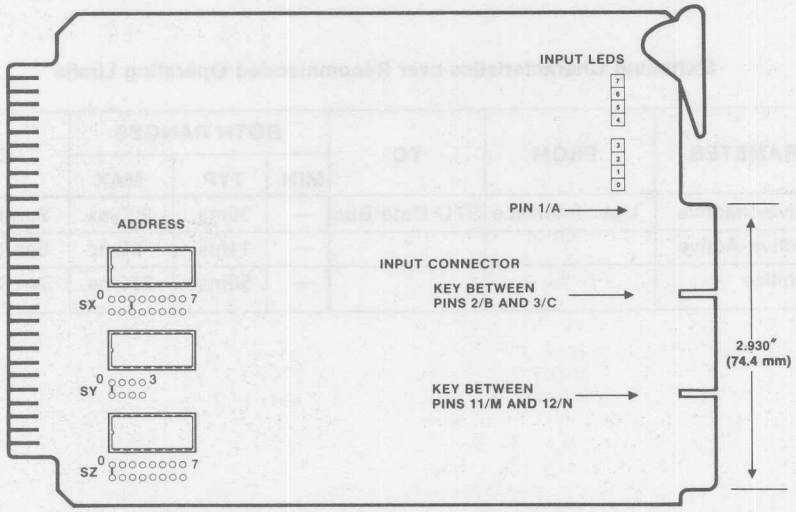
MECHANICAL

- Refer to the card address selection diagram for component placement information.
- The 7506 requires clearances of 0.150 in. (3.81mm) on the circuit side and 0.600 in. (15.24mm) on the component side of the printed circuit board when placed in a Series 7000 STD BUS Card Rack.
- Clear plastic shields are provided on both sides of the assembly for protection from high voltage. Both adjacent slots must be vacant for clearance of the input connector.

Interface Connector Information

See CB18 and CS18 data sheets for compatible connector information.

7506 OPTOISOLATED INPUT CARD



Card Address Selection

STD 7506 EDGE CONNECTOR PIN LIST								
PIN NUMBER					PIN NUMBER			
OUTPUT (LSTTL DRIVE)							OUTPUT (LSTTL DRIVE)	
INPUT (LSTTL LOADS)							INPUT (LSTTL LOADS)	
MNEMONIC								MNEMONIC
+5 V	VCC		2	1		VCC	+5 V
GROUND	GND		4	3		GND	GROUND
-5V			6	5			-5V
D7		55	8	7	55		D3
D6		55	10	9	55		D2
D5		55	12	11	55		D1
D4		55	14	13	55		D0
A15			16	15		1	A7
A14			18	17		1	A6
A13			20	19		1	A5
A12			22	21		1	A4
A11			24	23		1	A3
A10			26	25		1	A2
A9			28	27		1	A1
A8			30	29		1	A0
RD*	1		32	31			WR*
MEMRQ*			34	33		1	IORQ*
MEMEX			36	35		1	IOEXP
MCSYNC*			38	37			REFRESH*
STATUS 0*			40	39			STATUS 1*
BUSRQ*			42	41			BUSAK*
INTRQ*			44	43			INTAK*
NMIRQ*			46	45			WAITRQ*
PBRESET*			48	47			SYSRESET*
CNTRL*			50	49			CLOCK*
PCI	IN		52	51	OUT		PCO
AUX GND			54	53			AUX GND
AUX -V			56	55			AUX +V

*Active low level logic

Edge Connector Pin List

INTERFACE CONNECTOR PIN LIST 7506	
PIN NUMBER	SIGNAL
1/A	AC INPUT 7A
2/B	7B
3/C	AC INPUT 6A
4/D	6B
5/E	AC INPUT 5A
6/F	5B
7/H	AC INPUT 4A
8/J	4B
9/K	AC INPUT 3A
10/L	3B
11/M	AC INPUT 2A
12/N	2B
13/P	AC INPUT 1A
14/R	1B
15/S	AC INPUT 0A
16/T	0B
17/U	SPARE
18/V	SPARE

Interface Connector Pin LI

USER'S MANUAL

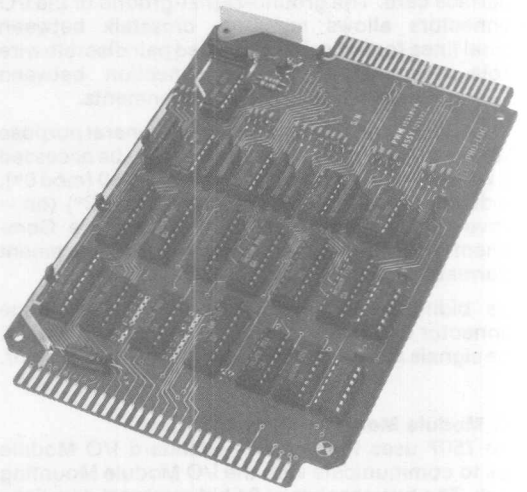
To obtain the user's manual for the 7506, ask for Pro-Log document #106678.

7000
STD BUS

7507
GENERAL PURPOSE INTERFACE CARD

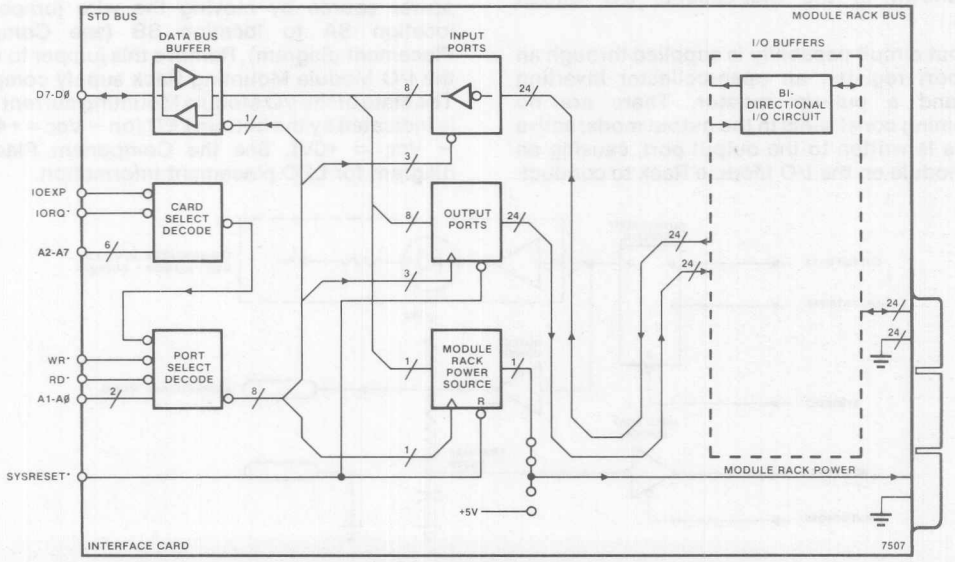
The 7507 is a general purpose TTL interface card. Three 8-bit read/write ports control 24 bidirectional signal lines. In addition, an output port-controlled power source rated at +4.7V at 500mA is provided. An LED assembly, visible from the card edge, monitors the state of the power source and the three signal lines. Connection to the 7507 is supplied through a 50-pin card edge connector. Adjacent grounds are provided for each signal line for use in ribbon cable or discrete wire cable assemblies.

The 7507 also provides an interface between the STD BUS and the Industry Standard I/O Module Mounting Rack (OPTO-22, Gordos, Crydom, Adatek or equivalent). This interface card can control up to 24 AC or DC input or output modules in any combination and position on the I/O Module Mounting Rack. The I/O Module Mounting Rack may be separated from the 7507 by up to ten feet (3m) of 50 conductor ribbon cable.



FEATURES

- **Up to 24 I/O modules per 7507**
- **Any type of module can be controlled in any combination and position**
- **Standard I/O module bus allows use of industry Standard industrial I/O module mounting racks**
- **500mA drive capability**
- **Low pass input filters for noisy industrial environments**
- **Single +5V operation**
- **Universal processor compatability—Z80, 8085, 6800, and others.**



7507 GENERAL PURPOSE INTERFACE CARD

FUNCTIONAL

General Purpose Interface

The 7507 is useful as a general purpose TTL interface card. The ground-signal-ground of the I/O connectors allows minimum crosstalk between signal lines for flat cable or twisted pair discrete wire cable assemblies for interconnection between systems in electrically noisy environments.

Three LED's are provided for use as general purpose status indicators. These indicators may be accessed by writing the output port bits for module 0 (mod 0*), module 1 (mod 1*), and module 2 (mod 2*) (on = active-high output register data). See the Component Placement diagram for LED placement information.

The bidirectional signal lines at the card edge connector are active-low on both input and output. The signals are terminated with a 1K pull-up resistor.

I/O Module Mounting Rack Interface

The 7507 uses the Industry Standard I/O Module Bus to communicate with the I/O Module Mounting Rack. The bus consists of 24 bidirectional data lines alternated with 24 ground lines, a switched +4.7V/500mA power lead and a ground power lead. These signals are routed over up to ten feet (3m) of 50-conductor flat cable.

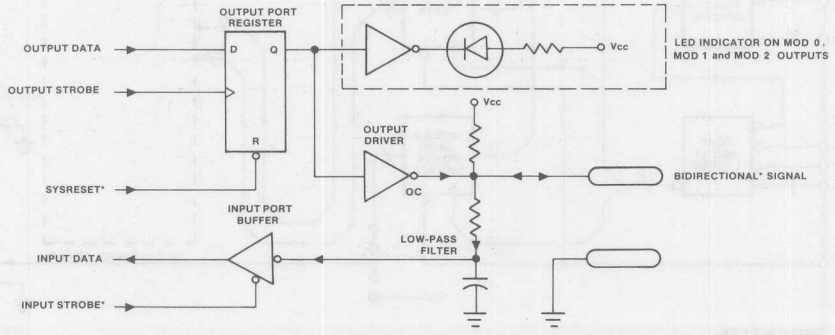
Each bidirectional data line controls one I/O module on the I/O Module Mounting Rack. Since the I/O module may be an input or an output device, each signal line must perform as an input or an output. This signal line characteristic is achieved by the circuit shown in the Bidirectional I/O Circuit diagram.

The output circuit capability is supplied through an output port register, an open-collector inverting driver, and a pull-up resistor. There are no programming constraints in the output mode; active high data is written to the output port, causing an output module on the I/O Module Rack to conduct.

Input circuit capability is provided through an inverting input port buffer and a low-pass RC filter. The low-pass filter, combined with the Schmitt-trigger characteristic of the input port buffer, removes noise-induced voltage spikes from the input signal. The active condition of any input module (high voltage present), appears as active-high data in the input port. There is one programming constraint in the input mode: active-high data cannot be written to the output port bit that is to be used on an input port bit. This constraint is required to disable the open-collector output drive for that bit. Note: On system power-up, the SYSRESET* signal clears the output port and puts the output drivers in the disabled state. Thus programming overhead is not required to select the input mode of operation.

The power needed to operate the I/O Module Mounting Rack is supplied by an output port-controlled power source capable of providing 500mA. To disable all input and output modules in the I/O Module Mounting Rack, this power source should be switched off by setting the I/O Module Rack power disable bit. This is useful when performing a test on the 7507. If the I/O Module Rack is disabled, the 7507 may be tested by writing a value to an output and then reading the value back for verification. A time delay is required before reading the value back to allow for the operation of the input filter. Check the Switching Characteristics table for the correct time delay value.

To output power directly from the Vcc of the STD system to the I/O Module Mounting Rack, it is possible to bypass the output port-controlled +4.7V power source by moving the wire jumper from location SA to location SB (see Component Placement diagram). Remove this jumper to disable the I/O Module Mounting Rack supply completely. The state of the I/O Module Mounting current supply is indicated by the bottom LED (on → Vcc = +4.7V, off → Vcc = +0V). See the Component Placement diagram for LED placement information.

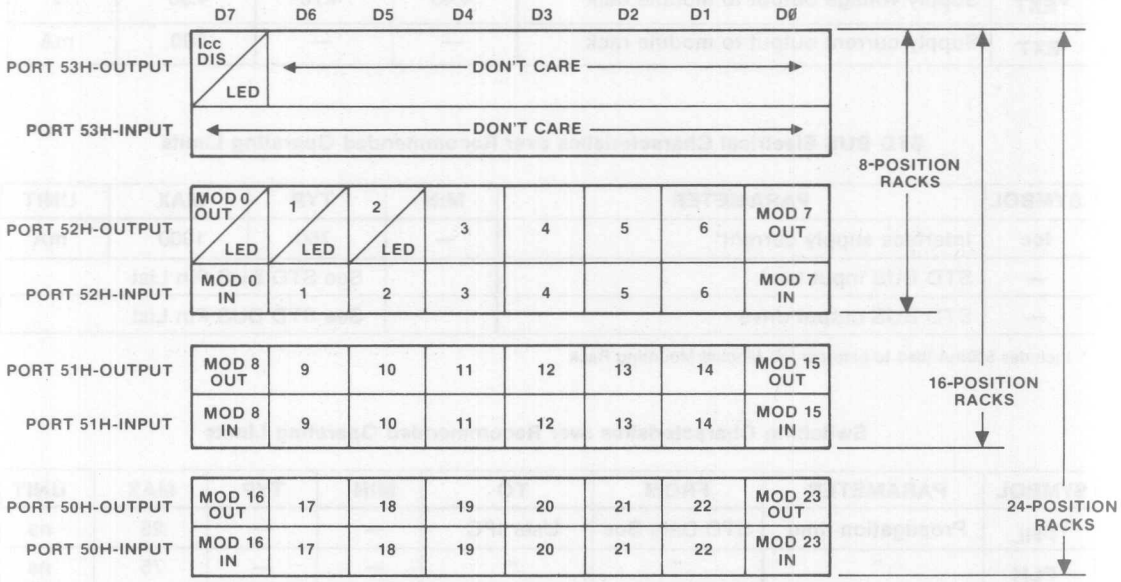


Typical Bidirectional I/O Circuit

Mapping

The 24 bidirectional signals are accessed as three 8-bit input/output ports. Note: The 24-position I/O Module Mounting Rack uses all three ports. The 16-position I/O Module Mounting Rack uses two ports. The 8-position rack requires a single input/output port. See the Port Mapping diagram for port assignments for all three configurations. The I/O Module Mounting Rack power supply uses the same 1-bit output-only port for all three I/O Module Rack configurations. With the exception of these differences, the three I/O configurations program identically.

The I/O ports of the 7507 are selected by a decoded combination of address lines A7 through A0. The 7507 is shipped with the port assignments shown in the Port Mapping diagram. For additional information, see *User's Manual.*



Port Mapping

ELECTRICAL

7507 I/O Module Mounting Rack Interface Card Electrical Specifications

SYMBOL	PARAMETER	RECOMMENDED OPERATING LIMITS			ABSOLUTE NONOPERATING LIMITS		
		MIN	TYP	MAX	MIN	MAX	UNIT
V_{CC}	Supply voltage	4.75	5.00	5.25	0.0	7.00	V
T_A	Free air temperature	0	25	55	-40	75	°C

User Interface Electrical Characteristics over Recommended Operating Limits

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{OL}	Low level interface voltage (at 10mA current level)	—	—	0.80	V
I_{OL}	Low level interface current (at 0.70V level)	—	—	20	mA
V_{OH}	High level interface voltage	4.75	—	5.25	V
I_{OH}	High level interface current (at 2.0V)	-3.0	—	—	mA
V_{EXT}	Supply voltage output to module rack	4.45	4.70	4.95	V
I_{EXT}	Supply current output to module rack	—	—	500	mA

STD BUS Electrical Characteristics over Recommended Operating Limits

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
Icc	Interface supply current*	—	750	1000	mA
—	STD BUS input load		See STD BUS Pin List		
—	STD BUS output drive		See STD BUS Pin List		

* Includes 500mA load to external I/O Module Mounting Rack

Switching Characteristics over Recommended Operating Limits

SYMBOL	PARAMETER	FROM	TO	MIN	TYP	MAX	UNIT
T_{PHL}	Propagation time	STD Data Bus	User IFC	—	—	25	ns
T_{PLH}	"	"	"	—	—	75	ns
T_{PHL}	Propagation time	User IFC	STD Data Bus	3	6	15	μs
T_{PLH}	"	"	"	3	6	15	μs

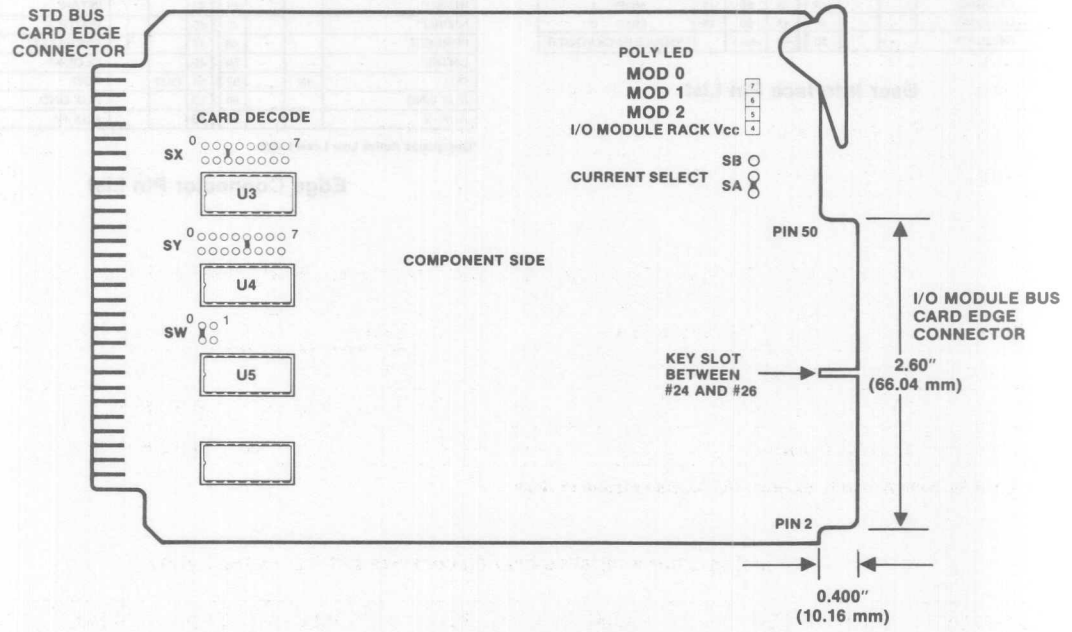
* Interface connector

MECHANICAL

Refer to the Component Placement diagram for component placement information. The 7507 meets all STD BUS general mechanical specifications. The 7507 requires one card slot in a standard STD BUS card rack. The input connector clearance requirements vary according to the specific connector used. A 50-pin flat cable connector requires clearances of 0.250 in. (6.35mm) on the component and circuit sides of the board.

Recommended flat cable card edge connectors include 3-M part number 3415-0001 or equivalent. This may be used with a polarizing key 3-M part number 3439-0000 or equivalent to avoid incorrect cable hook-up. A complete cable assembly may be obtained from Pro-Log as RC-50-6.

For discrete wire cable assemblies, a PC board edge connector with solder tail connections may be used in conjunction with a cable hood assembly to provide a reliable, strain relieved termination. The recommended 50-pin card edge connector is a Viking part number 3VH25/IJN5. This connector is used with a Viking Hood part number 036-0097-002 or equivalent.



Component Placement

7507 GENERAL PURPOSE INTERFACE CARD

7507 USER INTERFACE EDGE CONNECTOR PIN LIST							
PIN NUMBER				PIN NUMBER			
OUTPUT (LSTTL DRIVE)						OUTPUT (LSTTL DRIVE)	
INPUT (LSTTL LOADS)						INPUT (LSTTL LOADS)	
MNEMONIC						MNEMONIC	
GROUND			2	1	50	13	MOD 23
GROUND			4	3	50	13	MOD 22
GROUND			6	5	50	13	MOD 21
GROUND			8	7	50	13	MOD 20
GROUND			10	9	50	13	MOD 19
GROUND			12	11	50	13	MOD 18
GROUND			14	13	50	13	MOD 17
GROUND			16	15	50	13	MOD 16
GROUND			18	17	50	13	MOD 15
GROUND			20	19	50	13	MOD 14
GROUND			22	21	50	13	MOD 13
GROUND			24	23	50	13	MOD 12
GROUND			26	25	50	13	MOD 11
GROUND			28	27	50	13	MOD 10
GROUND			30	29	50	13	MOD 9
GROUND			32	31	50	13	MOD 8
GROUND			34	33	50	13	MOD 7
GROUND			36	35	50	13	MOD 6
GROUND			38	37	50	13	MOD 5
GROUND			40	39	50	13	MOD 4
GROUND			42	41	50	13	MOD 3
GROUND			44	43	50	13	MOD 2
GROUND			46	45	50	13	MOD 1
GROUND			48	47	50	13	MOD 0
GROUND			50	49	500mA		MODULE RACK POWER

User Interface Pin List

STD 7507 EDGE CONNECTOR PIN LIST							
PIN NUMBER				PIN NUMBER			
OUTPUT (LSTTL DRIVE)					OUTPUT (LSTTL DRIVE)		
INPUT (LSTTL LOADS)						INPUT (LSTTL LOADS)	
MNEMONIC						MNEMONIC	
+5 VOLTS	VCC		2	1		VCC	+5 VOLTS
GROUND	GND		4	3		GND	GROUND
-5V			6	5			-5V
D7	1	55	8	7	55	1	D3
D6	1	55	10	9	55	1	D2
D5	1	55	12	11	55	1	D1
D4	1	55	14	13	55	1	D0
A15			16	15		1	A7
A14			18	17		1	A6
A13			20	19		1	A5
A12			22	21		1	A4
A11			24	23		1	A3
A10			26	25		2	A2
A9			28	27		2	A1
A8			30	29		2	A0
RD*	1		32	31		1	WR*
MEMRQ*			34	33		1	IORQ*
MEMEX*			36	35		1	IOEXP*
MCSYNC*			38	37			REFRESH*
STATUS 0*			40	39			STATUS 1*
BUSRQ*			42	41			BUSAK*
INTRQ*			44	43			INTAK*
NMIRQ*			46	45			WAITRQ*
PBRESET*			48	47		1	SYSRESET*
CNTRL*			50	49			CLOCK*
PCI	IN		52	51	OUT		PCO
AUX GND			54	53			AUX GND
AUX -V			56	55			AUX +V

*Designates Active Low Level Logic

Edge Connector Pin List

USER'S MANUAL

To obtain the user's manual for the 7507, as for Pro-Log document #106394.

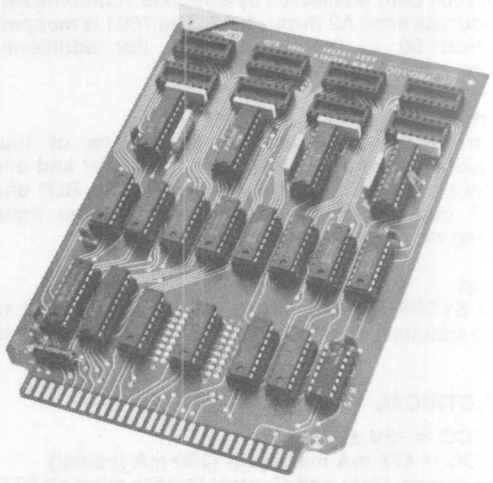
7000
STD BUS

7601
TTL INPUT/OUTPUT PORT CARD

This card provides four 8-bit gated input ports (32 (32 input lines) and four 8-bit latched output ports (32 output lines).

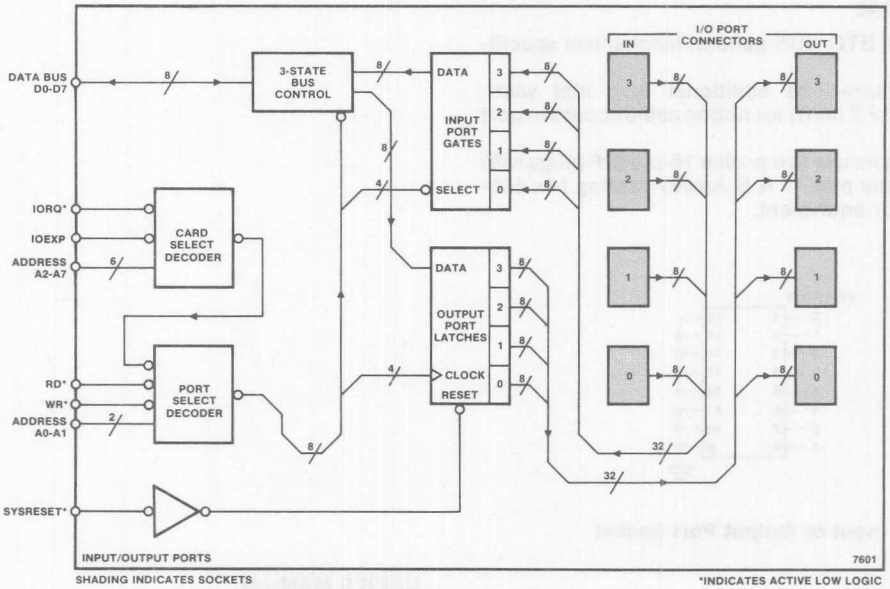
Input port lines and output port lines are accessed at 16-pin DIP sockets on the card. I/O lines are TTL-compatible with an input rating of 4 low-power Schottky TTL loads and an output drive rating of 20 low-power Schottky TTL loads (5 TTL loads). A reset line is available.

The 7601 decodes eight address lines with provision for expansion and memory mapping. An on-card jumper system allows the user to establish the four consecutive I/O port pair addresses occupied by the 7601.



FEATURES

- **User-selected port address (256-port field)**
- **Input rating: 4 LSTTL loads**
- **Output rating: 20 LSTTL loads (5 TTL loads)**
- **Provision for expansion and memory mapping**
- **Input buffers have 200 MV of hysteresis for additional noise margin**
- **Input lines include 4.7K pullup resistors**
- **Single +5V operation**
- **Universal processor compatibility—Z80, 8085, 6800, and others.**



7601 INPUT/OUTPUT PORT CARD

FUNCTIONAL

Card Address Mapping

The 7601 card is selected by a decoded combination of address lines A2 through A7. The 7601 is mapped at Port 00 to 03 hexadecimal. For additional information, see *User's Manual.*

Port Addresses

Address lines A0 and A1 select one of four sequential port addresses. One input port and one output port reside at each address. The RD* and WR* control inputs differentiate between input gating or output latch functions.

Reset

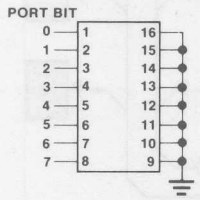
The SYSRESET* line clears all four output ports to zero simultaneously. The input ports are unaffected.

ELECTRICAL

- VCC = +5V ±5%
- ICC = 475 mA maximum (300 mA typical)
- Address, Data and Control Busses meet all STD BUS general electrical specifications
- Each input port line presents 4 LSTTL loads, and each output port line can drive 20 LSTTL loads
- 16-pin DIP sockets are provided for access to Input and Output Port bit lines. The diagram below shows the pin connections to these sockets for each port.

MECHANICAL

- Meets all STD BUS general mechanical specifications
- May require one additional card slot width [0.5 in. (12.7 mm)] for ribbon cable access to port sockets.
- Connectors use low profile 16-pin DIP plugs with heavy duty pins. T & B Ansley catalog No. 609-M165H or equivalent.



Input or Output Port Socket

STD/7601 EDGE CONNECTOR PIN LIST							
PIN NUMBER				PIN NUMBER			
OUTPUT (DRIVE)						OUTPUT (DRIVE)	
INPUT (LOADING)						INPUT (LOADING)	
MNEMONIC							MNEMONIC
+5V	VCC		2	1		VCC	+5V
GROUND	GND		4	3		GND	GROUND
-5V			6	5			-5V
D7	1	55	8	7	55	1	D3
D6	1	55	10	9	55	1	D2
D5	1	55	12	11	55	1	D1
D4	1	55	14	13	55	1	D0
A15			16	15		1	A7
A14			18	17		1	A6
A13			20	19		1	A5
A12			22	21		1	A4
A11			24	23		1	A3
A10			26	25		1	A2
A9			28	27		2	A1
A8			30	29		2	A0
RD*	1		32	31		1	WR*
MEMRQ*			34	33		1	IORQ*
MEMEX			36	35		1	IOEXP
MCSYNC*			38	37			REFRESH*
STATUS 0*			40	39			STATUS 1*
BUSRQ*			42	41			BUSAK*
INTRQ*			44	43			INTAK*
NMIRQ*			46	45			WAITRQ*
PBRESET*			48	47	1		SYSRESET*
CNTRL*			50	49			CLOCK*
PCI	IN		52	51	OUT		PCO
AUX GND			54	53			AUX GND
AUX -V			56	55			AUX +V

*Active low level logic

Edge Connector Pin List

USER'S MANUAL

To obtain the user's manual for the 7601, ask for Pro-Log document #106662.

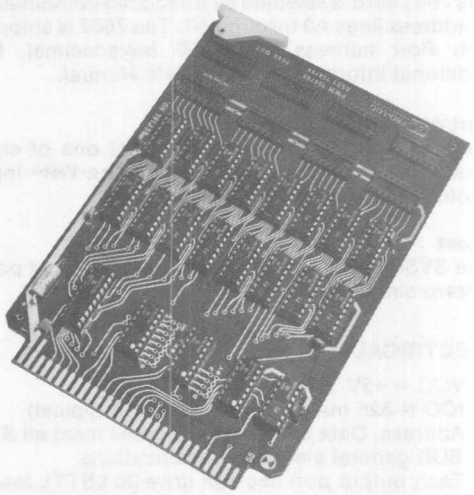
7000
STD BUS

7602
TTL OUTPUT PORT CARD

This card provides eight 8-bit latched output ports (64 output lines).

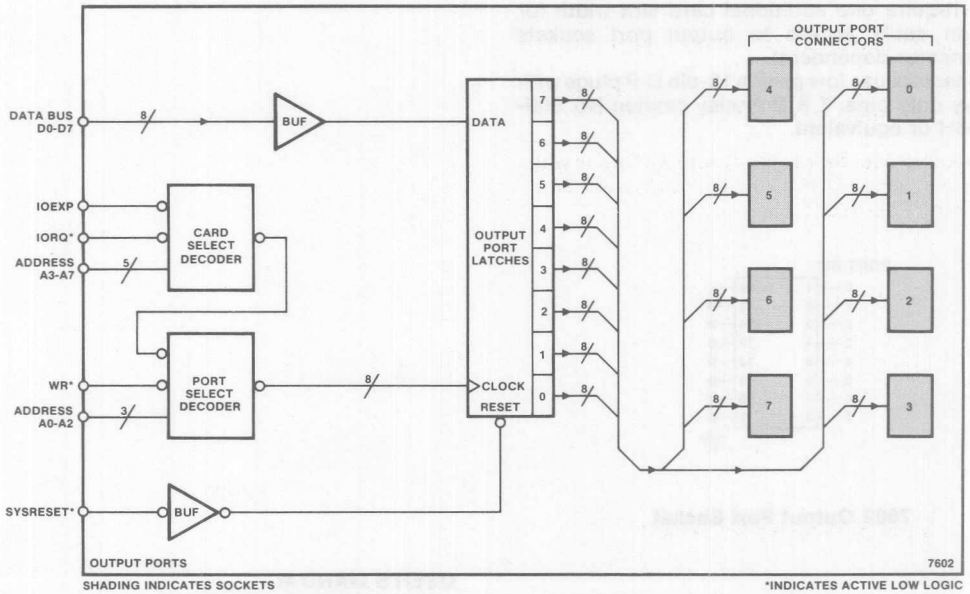
Output port lines are accessed at 16-pin DIP sockets on the card. The output lines are TTL-compatible with the ability to drive 20 low-power Schottky TTL loads each (5 TTL loads). A reset line is available to clear all ports simultaneously.

The 7602 decodes eight address lines with provision for expansion and memory mapping. An on-card jumper system allows the user to establish the eight consecutive output port addresses occupied by the 7602.



FEATURES

- **User-selectable port address (256-port field)**
- **Output drive: 20 low-power Schottky TTL loads**
- **Provision for expansion and memory mapping**
- **Single +5V operation**
- **Universal processor compatibility—Z80, 8085, 6800, and others.**



7602 OUTPUT PORT CARD

FUNCTIONAL

Card Address Mapping

The 7602 card is selected by a decoded combination of address lines A3 through A7. The 7602 is shipped with Port address 00 to 07 hexadecimal. For additional information, see *User's Manual.*

Port Addresses

Address lines A0, A1, and A2 select one of eight sequential output port addresses. The WR* input controls the output latch function.

Reset

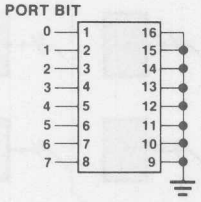
The SYSRESET* input clears all eight output ports to zero simultaneously.

ELECTRICAL

- VCC = +5V ±5%
- ICC = 325 mA maximum (210 mA typical)
- Address, Data and Control Busses meet all STD BUS general electrical specifications
- Each output port line can drive 20 LSTTL loads.
- 16-pin DIP sockets are provided for access to Output Port bit lines. The diagram below shows the pin connections to these sockets for each port.

MECHANICAL

- Meets all STD BUS general mechanical specifications
- May require one additional card slot width for ribbon cable access to output port sockets (connector-dependent).
- Connectors use low profile 16-pin DIP plugs with heavy duty pins. T & B Ansley catalog No. 609-M165H or equivalent.



7602 Output Port Socket

STD/7602 EDGE CONNECTOR PIN LIST							
PIN NUMBER	OUTPUT (DRIVE)	INPUT (LOADING)	MNEMONIC		PIN NUMBER	OUTPUT (DRIVE)	INPUT (LOADING)	MNEMONIC
+5V	VCC		2		1		VCC	+5V
GROUND	GND		4		3		GND	GROUND
-5V			6		5			-5V
D7	1	55	8		7	55	1	D3
D6	1	55	10		9	55	1	D2
D5	1	55	12		11	55	1	D1
D4	1	55	14		13	55	1	D0
A15			16		15		1	A7
A14			18		17		1	A6
A13			20		19		1	A5
A12			22		21		1	A4
A11			24		23		1	A3
A10			26		25		1	A2
A9			28		27		1	A1
A8			30		29		1	A0
RD*			32		31		1	WR*
MEMRQ*			34		33		1	IORQ*
MEMEX			36		35		1	IOEXP
MCSYNC*			38		37			REFRESH*
STATUS 0*			40		39			STATUS 1*
BUSRQ*			42		41			BUSAK*
INTRQ*			44		43			INTAK*
NMIRQ*			46		45			WAITRQ*
PBRESET*			48		47		1	SYSRESET*
CNTRL*			50		49			CLOCK*
PCI	IN		52		51	OUT		PCO
AUX GND			54		53			AUX GND
AUX -V			56		55			AUX +V

*Active low level logic

Edge Connector Pin List

USER'S MANUAL

To obtain the user's manual for the 7602, ask for Pro-Log document #106663.

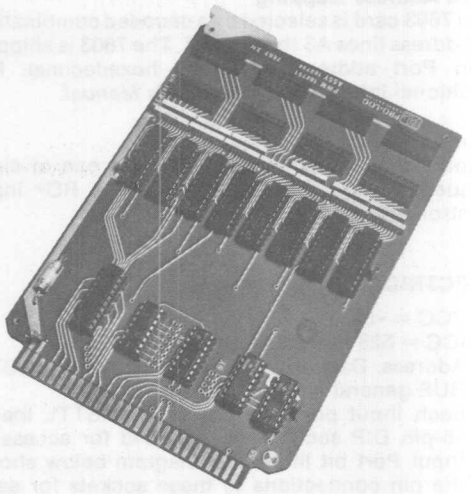
7000 STD BUS

7603 TTL INPUT PORT CARD

This card provides eight 8-bit gated input ports (64 (64 input lines).

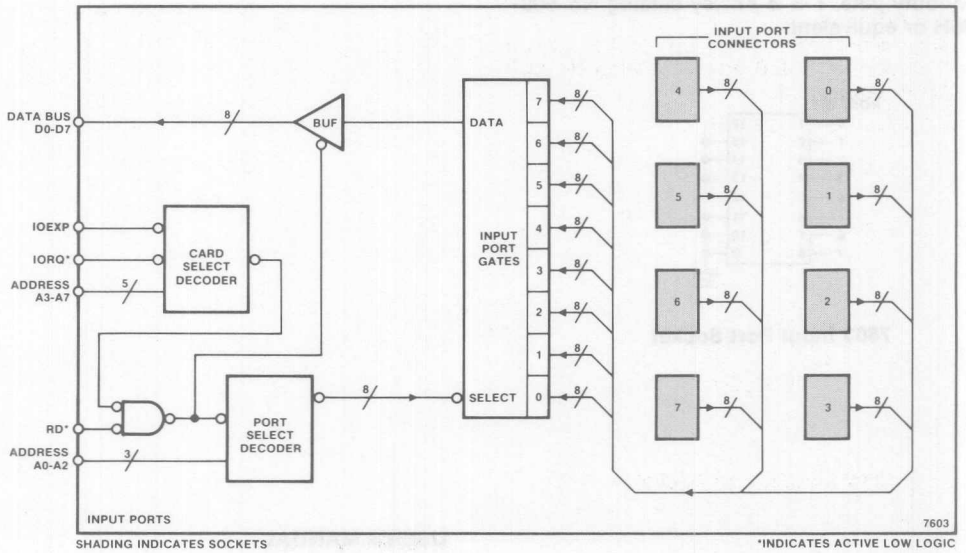
Input port lines are accessed at 16-pin DIP sockets on the card. The input lines are TTL-compatible with an input rating of 4 low-power Schottky TTL loads.

The 7603 decodes eight address lines with provision for expansion and memory mapping. An on-card jumper system allows the user to establish the eight consecutive input port addresses occupied by the 7603.



FEATURES

- **User-selectable port address (256-port field)**
- **Input rating of 4 low-power Schottky TTL loads**
- **Provision for expansion and memory mapping**
- **Input buffers have 200 MV of hysteresis**
- **Input lines include 4.7K pullups**
- **Single +5V operation**
- **Universal processor compatibility—Z80, 8085, 6800, and others.**



SHADING INDICATES SOCKETS

*INDICATES ACTIVE LOW LOGIC

7603 INPUT PORT CARD

FUNCTIONAL

Card Address Mapping

The 7603 card is selected by a decoded combination of address lines A3 through A7. The 7603 is shipped with Port address 00 to 07 hexadecimal. For additional information, see *User's Manual.*

Port Addresses

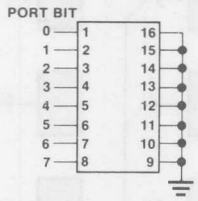
Address lines A0, A1, and A2 select one of eight sequential input port addresses. The RD* input controls the input gating function.

ELECTRICAL

- VCC = +5V ±5%
- ICC = 525 mA maximum (350 mA typical)
- Address, Data and Control Busses meet all STD BUS general electrical specifications
- Each input port line presents 4 LSTTL loads.
- 16-pin DIP sockets are provided for access to Input Port bit lines. The diagram below shows the pin connections to these sockets for each port.

MECHANICAL

- Meets all STD BUS general mechanical specifications
- May require one additional card slot width for ribbon cable access to output port sockets (connector-dependent).
- Connectors use low profile 16-pin DIP plugs with heavy duty pins. T & B Ansley catalog No. 609-M165H or equivalent.



7603 Input Port Socket

STD/7603 EDGE CONNECTOR PIN LIST							
PIN NUMBER				PIN NUMBER			
OUTPUT (DRIVE)						OUTPUT (DRIVE)	
INPUT (LOADING)							INPUT (LOADING)
MNEMONIC							MNEMONIC
+5V	VCC		2	1		VCC	+5V
GROUND	GND		4	3		GND	GROUND
-5V			6	5			-5V
D7		55	8	7	55		D3
D6		55	10	9	55		D2
D5		55	12	11	55		D1
D4		55	14	13	55		D0
A15			16	15		1	A7
A14			18	17		1	A6
A13			20	19		1	A5
A12			22	21		1	A4
A11			24	23		1	A3
A10			26	25		1	A2
A9			28	27		1	A1
A8			30	29		1	A0
RD*	1		32	31			WR*
MEMRQ*			34	33		1	IORQ*
MEMEX			36	35		1	IOEXP
MCSYNC*			38	37			REFRESH*
STATUS 0*			40	39			STATUS 1*
BUSRQ*			42	41			BUSAK*
INTRQ*			44	43			INTAK*
NMIRQ*			46	45			WAITRQ*
PBRESET*			48	47			SYSRESET*
CNTRL*			50	49			CLOCK*
PCI	IN		52	51	OUT		PCO
AUX GND			54	53			AUX GND
AUX -V			56	55			AUX +V

* Active low-level logic

Edge Connector Pin List

USER'S MANUAL

To obtain the user's manual for the 7603, ask for Pro-Log document #106664.

7000
STD BUS

7604
TTL INPUT/OUTPUT CARD

This card provides 8 ports of which any number can be input or output ports, or output ports with readback (64 I/O lines total).

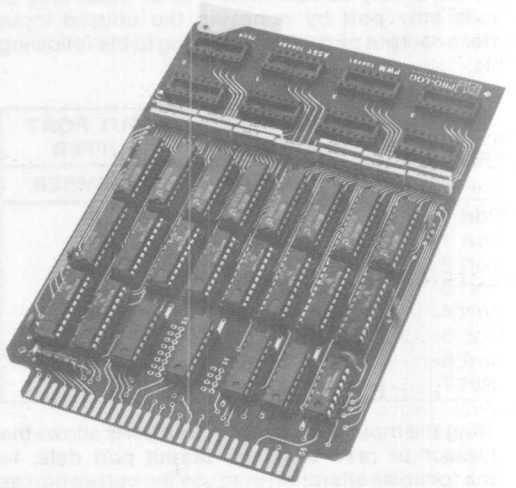
The ports are accessed at 16-pin DIP sockets on the card.

The output lines are TTL-compatible with the ability to drive 16 low-power Schottky TTL loads each (4 TTL loads). The system reset line clears all output ports simultaneously.

The input lines are TTL-compatible with an input rating of 4 low-power Schottky loads.

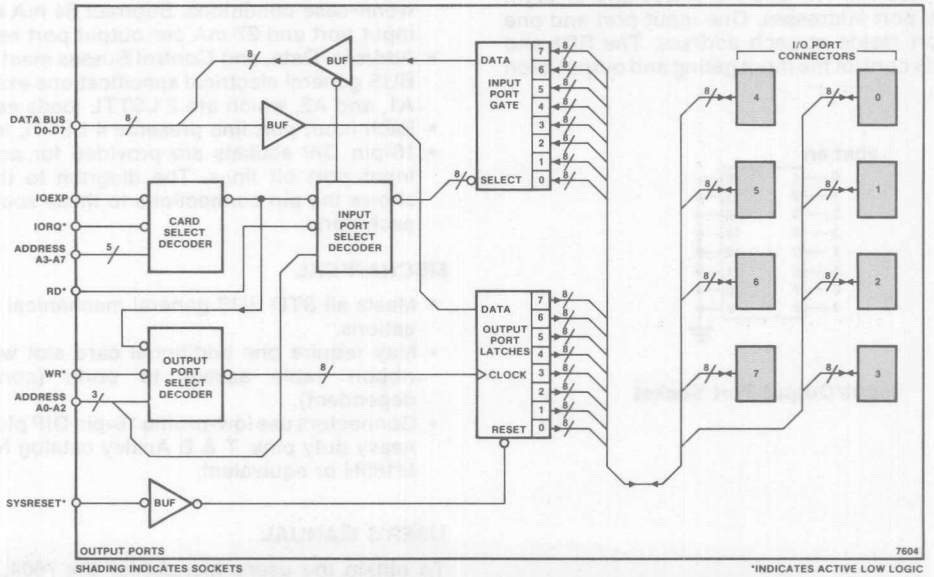
The ports may be configured as input only or output only ports simply by removing the unused IC associated with that port. If both IC's are retained, output port data may be read back into the processor through the input port.

The 7604 decodes eight address lines with provision for expansion and memory mapping. An on-card jumper system allows the user to establish the eight consecutive port addresses occupied by the 7604.



FEATURES

- **8 ports configurable as input or output, or output with readback**
- **User-selectable port address (256-port field)**
- **Outputs drive 16 low-power Schottky TTL loads**
- **Provision for expansion and memory mapping**
- **Single +5V operation**
- **Universal processor compatibility—Z80, 8085, 6800, and others.**



7604 TTL I/O CARD

FUNCTIONAL

The 7604 is shipped fully populated. Each of the eight ports may be customized as an input only or output only port by removing the unused input buffer or output port latch according to the following table.

PORT NO.	OUTPUT PORT LATCH	INPUT PORT BUFFER
	IC NUMBER	IC NUMBER
Port 0	U17	U9
Port 1	U19	U11
Port 2	U21	U13
Port 3	U23	U15
Port 4	U16	U8
Port 5	U18	U10
Port 6	U20	U12
Port 7	U22	U14

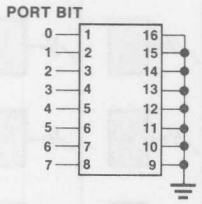
Leaving the input buffer in at output ports allows the processor to read back the output port data, to check for noise alteration or to use the output port as a data register.

Card Address Mapping

The 7604 card is selected by a decoded combination of address lines A3 through A7. The 7604 is shipped with port address 00 hexadecimal. For additional information, see *User's Manual.*

Port Addresses

Address lines A0, A1, and A2 select one of eight sequential port addresses. One input port and one output port reside at each address. The RD* and WR* inputs control the input gating and output latch functions.



Input/Output Port Socket

STD/7604 EDGE CONNECTOR PIN LIST							
PIN NUMBER	OUTPUT (DRIVE)	INPUT (LOADING)	MNEMONIC	PIN NUMBER	OUTPUT (DRIVE)	INPUT (LOADING)	MNEMONIC
+5V	VCC		2	1		VCC	+5V
GROUND	GND		4	3		GND	GROUND
-5V			6	5			-5V
D7	1	55	8	7	55	1	D3
D6	1	55	10	9	55	1	D2
D5	1	55	12	11	55	1	D1
D4	1	55	14	13	55	1	D0
A15			16	15		1	A7
A14			18	17		1	A6
A13			20	19		1	A5
A12			22	21		1	A4
A11			24	23		1	A3
A10			26	25		2	A2
A9			28	27		2	A1
A8			30	29		2	A0
RD*	1		32	31		1	WR*
MEMRQ*			34	33		1	IORQ*
MEMEX			36	35		1	IOEXP
MCSYNC*			38	37			REFRESH*
STATUS 0*			40	39			STATUS 1*
BUSRQ*			42	41			BUSAK*
INTRQ*			44	43			INTAK*
NMIRQ*			46	45			WAITRQ*
PBRESET*			48	47		1	SYSRESET*
CNTRL*			50	49			CLOCK*
PCI	IN		52	51	OUT		PCO
AUX GND			54	53			AUX GND
AUX -V			56	55			AUX +V

*Active low level logic

Edge Connector Pin List

ELECTRICAL

- VCC = +5V ±5%
- ICC = 700 mA maximum (450 mA typical) for worst-case conditions. Subtract 54 mA max per input port and 27 mA per output port removed.
- Address, Data, and Control Busses meet all STD BUS general electrical specifications except A0, A1, and A2, which are 2 LSTTL loads each.
- Each input port line presents 4 LSTTL loads.
- 16-pin DIP sockets are provided for access to input port bit lines. The diagram to the right shows the pin connections to these sockets for each port.

MECHANICAL

- Meets all STD BUS general mechanical specifications.
- May require one additional card slot width for ribbon cable access to ports (connector-dependent).
- Connectors use low-profile 16-pin DIP plugs with heavy duty pins. T & B Ansley catalog No. 609-M165H or equivalent.

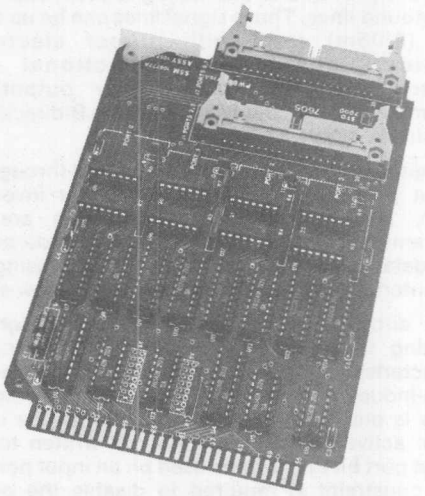
USER'S MANUAL

To obtain the user's manual for the 7604, ask for Pro-Log document #106665.

7000
STD BUS

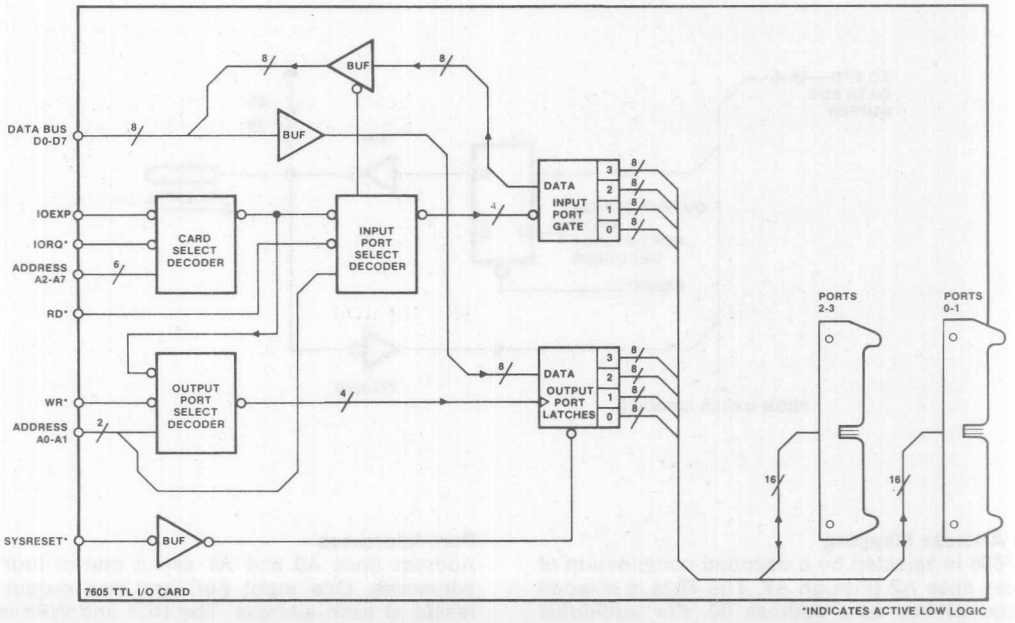
7605
PROGRAMMABLE TTL I/O CARD

The 7605 supplies four 8-bit I/O ports that can be programmed as input, output, or output with readback (total of 32 programmable I/O lines). The ports are accessed by two 40-pin latched connectors with 0.025 inch (0.635 mm) post headers. The output lines are TTL-compatible open-collector drivers with 1K pullups. These lines are tied to input ports. After power-on reset, all ports are in input mode. To use an output port, the user simply writes to the port lines desired. The 7605 decodes eight address lines with provision for expansion. An on-card jumper system allows the user to map the four consecutive port addresses occupied by the 7605 anywhere on four port boundaries in the 256-port address field.



FEATURES

- **32 I/O lines, each programmable as input, output, or output with readback**
- **User-selectable port address (256-port field)**
- **Single +5V operation**
- **Uses two latching 40-pin headers**
- **Input port loading 14 LSTTL loads**
- **Output can drive 50 LSTTL loads**
- **Available in inverted/noninverted outputs**
- **Universal processor compatibility—Z80, 8085, 6800, and others.**



7605 PROGRAMMABLE TTL I/O CARD

FUNCTIONAL

The 7605 provides 32 alternating bidirectional data and ground lines. These signal lines can be up to 10 feet (3.05m) long with proper electrical considerations. Each bidirectional line characteristic (whether input or output) is determined by the circuit shown in the Bidirectional I/O Circuit diagram.

The output circuit capability is supplied through an output port resistor, an open-collector inverting driver, and a pullup resistor. There are no programming constraints in the output mode; active high data is written to the output port, causing the user interface pin to operate in the active low state.

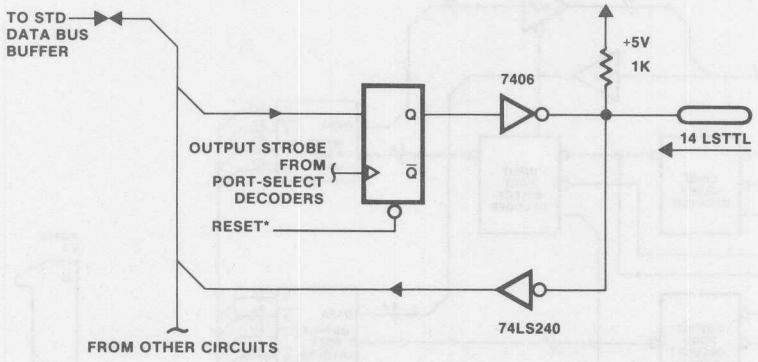
Input circuit capability is provided through an inverting input port buffer. The Schmitt-trigger characteristic of the input port buffer removes noise-induced voltage spikes from the input signal. There is one programming constraint in the input mode: active-high data cannot be written to the output port bit that is to be used on an input port bit. This constraint is required to disable the open-collector output drive for that bit. NOTE: On system power-up the SYSRESET* signal clears the output port and places the output drivers in the disabled state. Thus programming overhead is not required to select the input mode of operation.

Vcc is provided on the user interface pins J1 and J2. These should be used only after the system designer has thoroughly studied the system implication. Care must be taken to avoid ground loops.

The 7605 is shipped fully populated. Power dissipation can be reduced by removing unused input or output ports by removing the ICs:

INPUT/OUTPUT PORT SELECTION		
PORT NO.	**INPUT PORT REMOVE ICs**	**OUTPUT PORT REMOVE IC**
PORT 0	U7, U15, U19	U8
PORT 1	U9, U16, U20	U10
PORT 2	U11, U17, U21	U12
PORT 3	U13, U18, U22	U14

Leaving the input buffers in place allows the processor to read back the output port data, to check for noise alteration or to use the output port as a data register.

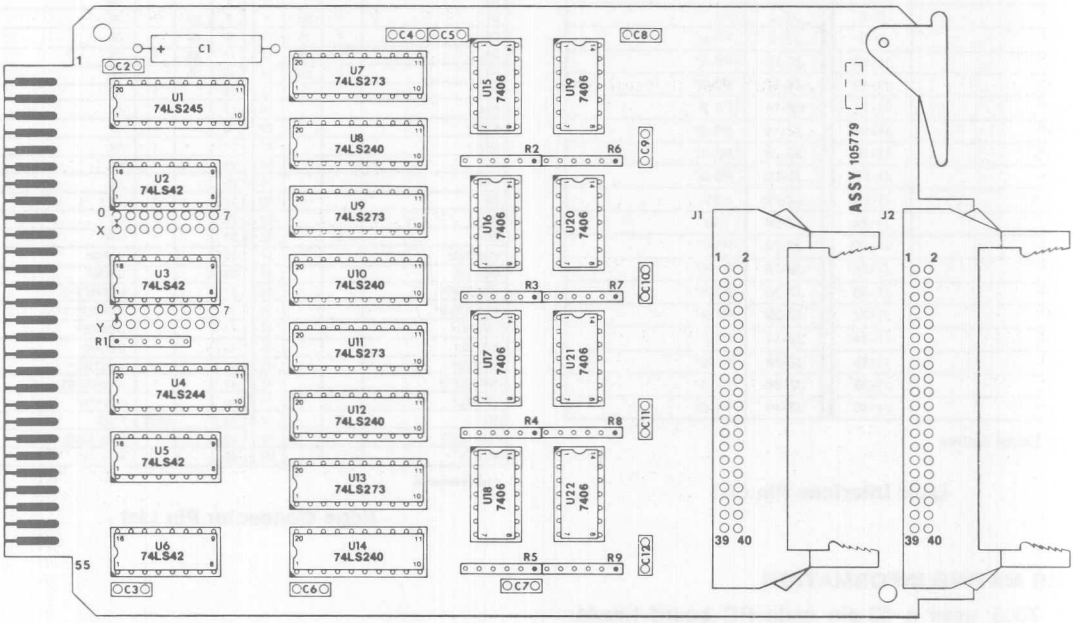


Card Address Mapping

The 7605 is selected by a decoded combination of address lines A2 through A7. The 7605 is shipped mapped at hex port address 00. For additional information, see *User's Manual.*

Port Addresses

Address lines A0 and A1 select one of four port addresses. One input port and one output port reside at each address. The RD* and WR* inputs control the input gating and output latch functions.



7605 Assembly

ELECTRICAL

- Vcc = +5V ±5%
- Icc = 800mA maximum (680mA typical). For worst-case conditions, subtract 55mA maximum per port configured as an input port, and subtract 35mA maximum per port configured as an output port.
- Address, Data, and Control buses meet all STD BUS general electrical specifications.
- Each input port line supplies 14 LSTTL loads.
- The User Interface Connector Pin List table shows the pin connections to these sockets for each port.
- Timing: Meets the specifications given in Section 2 of the STD Manual, for TTL input/output card timing.

MECHANICAL

- Meets all STD BUS general mechanical specifications.
- Connectors use low-profile, mass termination 0.025 inch (0.635 mm) post latching connectors (see the 7605 Assembly drawing and the User Interface Connector Pin List).
- Pro-Log Cables RC704-1 and RC704-2 are compatible with this card.

7605 PROGRAMMABLE TTL I/O CARD

7605 USER INTERFACE CONNECTOR PIN LIST			
CONNECTOR J1		CONNECTOR J2	
PIN NUMBER		PIN NUMBER	
SIGNAL			SIGNAL
-5V	J1-2	J2-2	-5V
-5V	J1-4	J2-4	-5V
P2-7*	J1-6	J2-6	P0-7*
P2-6*	J1-8	J2-8	P0-6*
P2-5*	J1-10	J2-10	P0-5*
P2-4*	J1-12	J2-12	P0-4*
P2-3*	J1-14	J2-14	P0-3*
P2-2*	J1-16	J2-16	P0-2*
P2-1*	J1-18	J2-18	P0-1*
P2-0*	J1-20	J2-20	P0-0*
-5V	J1-22	J2-22	-5V
-5V	J1-24	J2-24	-5V
P3-7*	J1-26	J2-26	P1-7*
P3-6*	J1-28	J2-28	P1-6*
P3-5*	J1-30	J2-30	P1-5*
P3-4*	J1-32	J2-32	P1-4*
P3-3*	J1-34	J2-34	P1-3*
P3-2*	J1-36	J2-36	P1-2*
P3-1*	J1-38	J2-38	P1-1*
P3-0**	J1-40	J2-40	P1-0*

*Low Level Active

User Interface Pin List

STD/7605 EDGE CONNECTOR PIN LIST							
PIN NUMBER				PIN NUMBER			
OUTPUT (LSTTL DRIVE)						OUTPUT (LSTTL DRIVE)	
INPUT (LSTTL LOADS)						INPUT (LSTTL LOADS)	
MNEMONIC							MNEMONIC
+5V	VCC		2	1		VCC	+5V
GROUND	GND		4	3		GND	GROUND
-5V			6	5			-5V
D7	1	55	8	7	55	1	D3
D6	1	55	10	9	55	1	D2
D5	1	55	12	11	55	1	D1
D4	1	55	14	13	55	1	D0
A15			16	15		1	A7
A14			18	17		1	A6
A13			20	19		1	A5
A12			22	21		1	A4
A11			24	23		1	A3
A10			26	25		2	A2
A9			28	27		2	A1
A8			30	29		2	A0
RD*	1		32	31		1	WR*
MEMRQ*			34	33		1	IORQ*
MEMEX			36	35		1	IOEXP
MCSYNC*			38	37			REFRESH*
STATUS 0*			40	39			STATUS 1*
BUSRQ*			42	41			BUSAK*
INTRQ*			44	43			INTAK*
NMIRQ*			46	45			WAITRQ*
PBRESET*			48	47		1	SYSRESET*
CNTRL*			50	49			CLOCK*
PCI	IN		52	51		OUT	PCO
AUX GND			54	53			AUX GND
AUX -V			56	55			AUX +V

* Active low-level logic

Edge Connector Pin List

USER MATING INFORMATION

The 7605 uses a 40-pin male PC board header connector (3M PN 3432-130 or equivalent). The matching female socket for use in standard flat cable applications is 3M PN 3417-6040.

ORDERING INFORMATION

7605-0: Inverted outputs
7605-1: Noninverted outputs

USER'S MANUAL

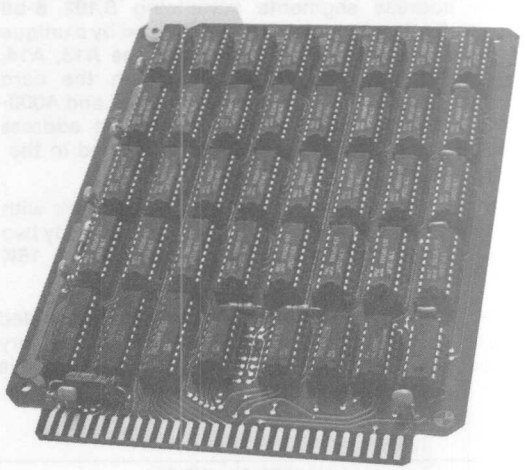
To obtain the user's manual for the 7605, ask for Pro-Log document #106666.

7701 MEMORY CARD

16K BYTE STATIC RAM MEMORY CARD

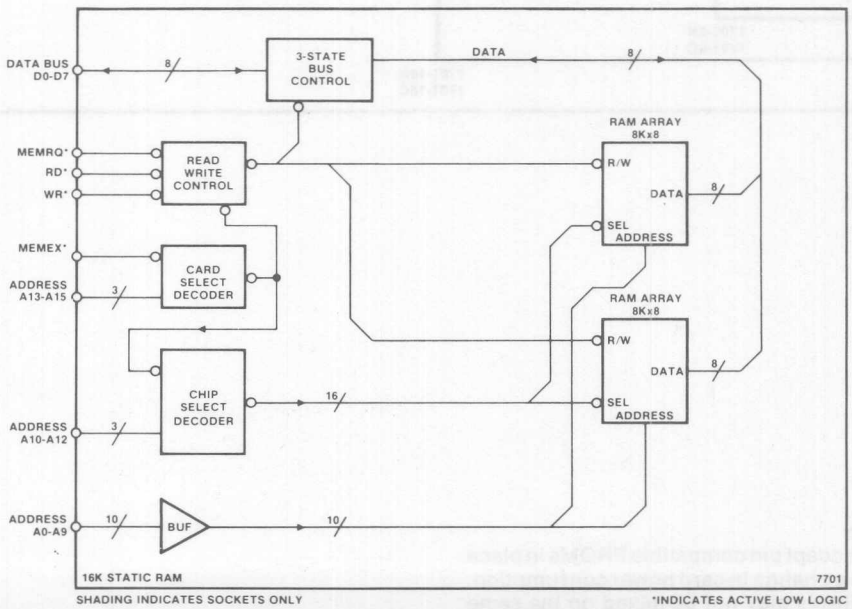
This card provides sockets for up to 16,384 bytes of Read-Write or PROM memory. The card uses type 2114 and type 6514 RAMs or equivalent and has sockets for 16 pairs of RAMs. Alternately, the card accepts pin-compatible PROMs or equivalent. PROMs and RAMs can not be mixed on the same card.

The 7701 decodes 16 address lines and can be mapped into either 8K or 16K bytes of consecutive address space. An on-card jumper system allows users to establish which 8K or 16K segment of a 64K microprocessor memory each 7701 occupies.



FEATURES

- **Sockets for 16K bytes of type 2114L RAMs, type 6514 RAMs, or pin-compatible PROMs**
- **User-selectable card address**
- **All STD BUS lines buffered**
- **Minimal logic bus loading**
- **Single +5V operation**
- **475ns access time with type 2114L RAMs**
- **275ns access time with type 6514-1 RAMs**
- **Low-power CMOS option (750mW typical)**
- **Universal processor compatibility—Z80, 8085, 6800, and others.**



SHADING INDICATES SOCKETS ONLY

*INDICATES ACTIVE LOW LOGIC

7701, MEMORY CARDS

FUNCTIONAL

Card Address Mapping

The 7701 is organized as two blocks of consecutive RAM address segments containing 8,192 8-bit words. Each segment of RAM is enabled by a unique decoded combination of address lines A13, A14, and A15. The 7701 is shipped with the card responding to Hex addresses 8000-9FFF and A000-BFFF. To map the card at a different address segment, use mapping scheme as defined in the *User's Manual.*

The card can occupy one 8K address block with only one select line connected, or it can occupy two separate 8K blocks or a single consecutive 16K block.

Note that the card's data bus drivers are enabled anytime a valid address is present, even if memory chips are not plugged in. The card address range is chosen to prevent bus contention with other system memory elements, including Processor on-card memory, other memory cards, and memory-mapped I/O.

Plug-in RAMs

Sockets are provided for thirty-two 1Kx4 RAM devices. Each pair of these 1024x4 devices adds 1K 8-bit bytes of RAM, which are designated Memory Blocks 0-7 (MB0-MB7). Insert the RAMs to add memory according to the following table. If the memory card mapping is changed, use the table below, and the Memory Address Map and Jumper Selection for 1K memory blocks, to determine the new address range of each memory block.

MAPPED BY LINE SX						MAPPED BY LINE SY					
RAM SOCKETS	MEMORY BLOCK	ADR RANGE AS SHIPPED	RAM SOCKETS	MEMORY BLOCK	ADR RANGE AS SHIPPED	RAM SOCKETS	MEMORY BLOCK	ADR RANGE AS SHIPPED	RAM SOCKETS	MEMORY BLOCK	ADR RANGE AS SHIPPED
U9, U17	MB0	8000-83FF	U13, U21	MB4	9000-93FF	U25, U33	MB0	A000-A3FF	U29, U37	MB4	B000-B3FF
U10, U18	MB1	8400-87FF	U14, U22	MB5	9400-97FF	U26, U34	MB1	A400-A7FF	U30, U38	MB5	B400-B7FF
U11, U19	MB2	8800-8BFF	U15, U23	MB6	9800-9BFF	U27, U35	MB2	A800-ABFF	U31, U39	MB6	B800-BBFF
U12, U20	MB3	8C00-8FFF	U16, U24	MB7	9C00-9FFF	U28, U36	MB3	AC00-AFFF	U32, U40	MB7	BC00-BFFF
7701-4N 7701-4C											
7701-8N 7701-8C											
7701-16N 7701-16C											

PROM Option

The 7701 will accept pin compatible PROMs in place of RAMs, with a change in card power consumption. PROMs and RAMs may not be mixed on the same card.

ELECTRICAL

- VCC = +5V ±5%
- ICC = 2.28A maximum (1.6A typical) with NMOS RAM sockets fully loaded (65 mA max per NMOS RAM).
- ICC = 0.28A maximum (0.15A typical) with CMOS RAM sockets fully loaded.
- Address, data, and control buses meet all STD BUS general electrical specifications, except: A10, A11, A12—these address bus inputs present 2 LSTTL loads maximum each.

MECHANICAL

- Meets all STD BUS general mechanical specifications.

STD 7701 EDGE CONNECTOR PIN LIST							
PIN NUMBER				PIN NUMBER			
OUTPUT (DRIVE)				OUTPUT (DRIVE)			
INPUT (LOADING)							INPUT (LOADING)
MNEMONIC							MNEMONIC
+5 VOLTS	VCC		2	1		VCC	+5 VOLTS
GROUND	GND		4	3		GND	GROUND
-5VOLTS			6	5			-5VOLTS
D7	1	55	8	7	55	1	D3
D6	1	55	10	9	55	1	D2
D5	1	55	12	11	55	1	D1
D4	1	55	14	13	55	1	D0
A15	1		16	15		1	A7
A14	1		18	17		1	A6
A13	1		20	19		1	A5
A12	2		22	21		1	A4
A11	2		24	23		1	A3
A10	2		26	25		1	A2
A9	1		28	27		1	A1
A8	1		30	29		1	A0
RD*	1		32	31		1	WR*
MEMRQ*	1		34	33			IORC*
MEMEX*	1		36	35			IOEXP*
MCSYNC*			38	37			REFRESH*
STATUS 0*			40	39			STATUS 1*
BUSRQ*			42	41			BUSAK*
INTRQ*			44	43			INTAK*
NMIRQ*			46	45			WAITRQ*
PBRESET*			46	47			SYSRESET*
CNTRL*			50	49			CLOCK*
PC1	IN		52	51	OUT		PC0
AUX GND			54	53			AUX GND
AUX -V			56	55			AUX +V

* Active low level logic

Edge Connector Pin List

ORDERING INFORMATION FOR STANDARD CONFIGURATIONS

The 770l is available in the following configuration:

7701	— No memory chips supplied, sockets only for 16K of RAM.
7701-4N	— 4K of 2114L NMOS RAMs preinstalled and tested.
7701-8N	— 8K of 2114L NMOS RAMs preinstalled and tested.
7701-16N	— 16K of 2114L NMOS RAMs preinstalled and tested.
7701-4C	— 4K of 6514 CMOS RAMs preinstalled and tested.
7701-8C	— 8K of 6514 CMOS RAMs preinstalled and tested.
7701-16C	— 16K of 6514 CMOS RAMs preinstalled and tested.

USER'S MANUAL

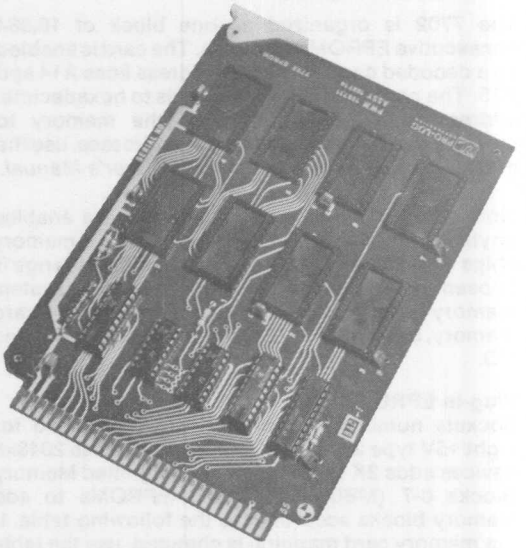
To obtain the user's manual for the 7701, ask for Pro-Log document #106690.

7702 MEMORY CARDS

16K BYTE 2716 EPROM MEMORY CARD

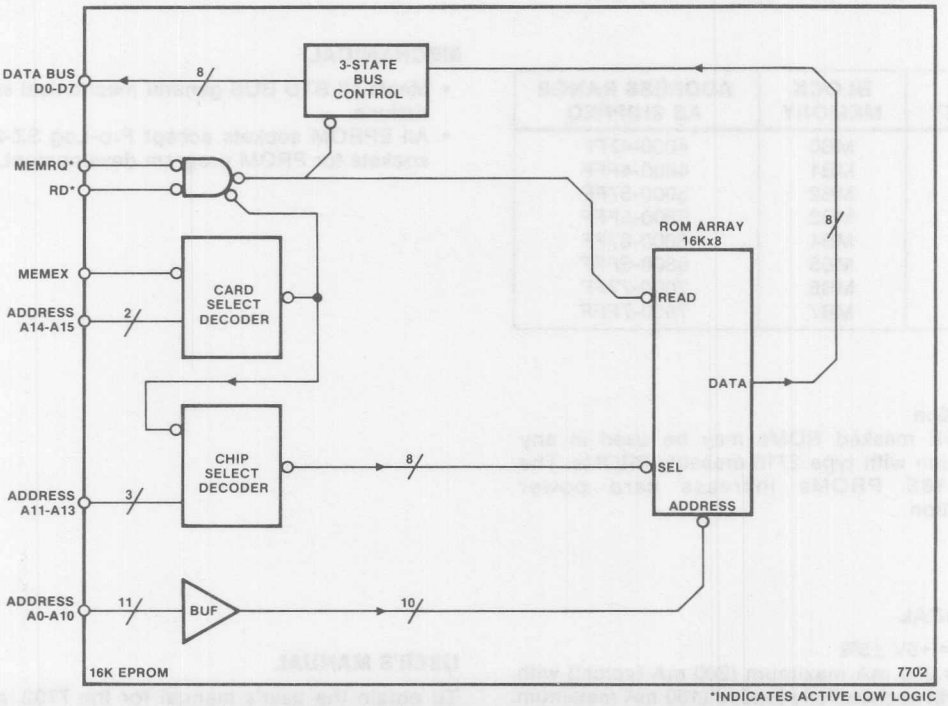
This card provides sockets for up to 16,384 bytes of EPROM memory. The card uses type 2716 EPROMs or equivalent and has sockets for 8 EPROMs.

The 7702 decodes 16 address lines and occupies 16K consecutive addresses. An on-card jumper system allows users to establish which quadrant of a 64K microprocessor memory each 7702 occupies.



FEATURES

- **Sockets for 16K bytes ROM (type 2716 EPROMs)**
- **User-selectable card address**
- **All STD BUS lines buffered**
- **Minimal logic bus loading**
- **Single +5V operation**
- **Uses Pro-Log D2002 2Kx8 EPROMs**
- **Universal processor compatibility—Z80, 8085, 6800, and others.**



*INDICATES ACTIVE LOW LOGIC

FUNCTIONAL

Card Address Mapping

The 7702 is organized as one block of 16,384 consecutive EPROM addresses. The card is enabled by a decoded combination of address lines A14 and A15. The card as shipped responds to hexadecimal addresses 4000-7FFF. To map the memory to respond to a different segment of addresses, use the mapping scheme as defined in the *User's Manual.*

Note that the card's data bus drivers are enabled anytime a valid address is present, even if memory chips are not plugged in. The card address range is chosen to prevent bus contention with other system memory elements, including processor on-card memory, other memory cards, and memory-mapped I/O.

Plug-in EPROMs

Sockets numbered 0 through 7 are provided for eight +5V type 2716 EPROMs. Each of these 2048x8 devices adds 2K bytes of ROM, designated Memory Blocks 0-7 (MB0-MB7). Insert EPROMs to add memory blocks according to the following table. If the memory card mapping is changed, use the table below, the Memory Address Map and Jumper Selection Table for 2K memory blocks, to determine the new address range of each memory block.

ROM SOCKET	BLOCK MEMORY	ADDRESS RANGE AS SHIPPED
0	MB0	4000-47FF
1	MB1	4800-4FFF
2	MB2	5000-57FF
3	MB3	5800-5FFF
4	MB4	6000-67FF
5	MB5	6800-6FFF
6	MB6	7000-77FF
7	MB7	7800-7FFF

ROM Option

The 2316E masked ROMs may be used in any combination with type 2716 erasable PROMs. The type 2316E PROMs increase card power consumption.

ELECTRICAL

- VCC = +5V ±5%
- ICC = 300 mA maximum (200 mA typical) with EPROM sockets fully loaded (100 mA maximum per EPROM selected, 25 mA standby).

STD/7702 EDGE CONNECTOR PIN LIST							
PIN NUMBER	OUTPUT (DRIVE)	INPUT (LOADING)	MNEMONIC	PIN NUMBER	OUTPUT (DRIVE)	INPUT (LOADING)	MNEMONIC
+5V	VCC		2	1		VCC	+5V
GROUND	GND		4	3		GND	GROUND
-5V			6	5			-5V
D7		55	8	7	55		D3
D6		55	10	9	55		D2
D5		55	12	11	55		D1
D4		55	14	13	55		D0
A15	1		16	15		1	A7
A14	1		18	17		1	A6
A13	1		20	19		1	A5
A12	1		22	21		1	A4
A11	1		24	23		1	A3
A10	1		26	25		1	A2
A9	1		28	27		1	A1
A8	1		30	29		1	A0
RD*	1		32	31			WR*
MEMRQ*	1		34	33			IORQ*
MEMEX	1		36	35			IOEXP
MCSYNC*			38	37			REFRESH*
STATUS 0*			40	39			STATUS 1*
BUSRQ*			42	41			BUSAK*
INTRQ*			44	43			INTAK*
NMIRQ*			46	45			WAITRQ*
PBRESET*			48	47			SYSRESET*
CNTRL*			50	49			CLOCK*
PCI	IN		52	51	OUT		PCO
AUX GND			54	53			AUX GND
AUX -V			56	55			AUX +V

* Active low-level logic

Edge Connector Pin List

MECHANICAL

- Meets all STD BUS general mechanical specifications.
- All EPROM sockets accept Pro-Log SZ-24 ZIF sockets for PROM program development.

USER'S MANUAL

To obtain the user's manual for the 7702, ask for Pro-Log document #106965.

7000 STD BUS

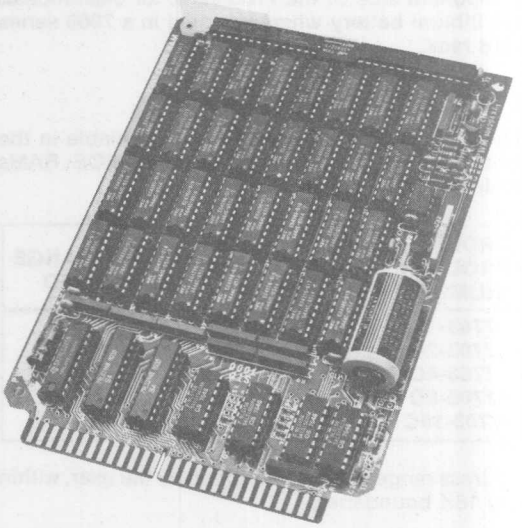
7703

BATTERY-BACKED CMOS RAM CARD

The 7703 card provides up to 16,384 bytes of high-speed (250ns), nonvolatile static CMOS RAM. It has a lithium battery backup that allows it to retain data for a minimum of two years; also, it generates a low-battery status signal (with an LED indicator) that may be jumpered to the STD nonmaskable interrupt.

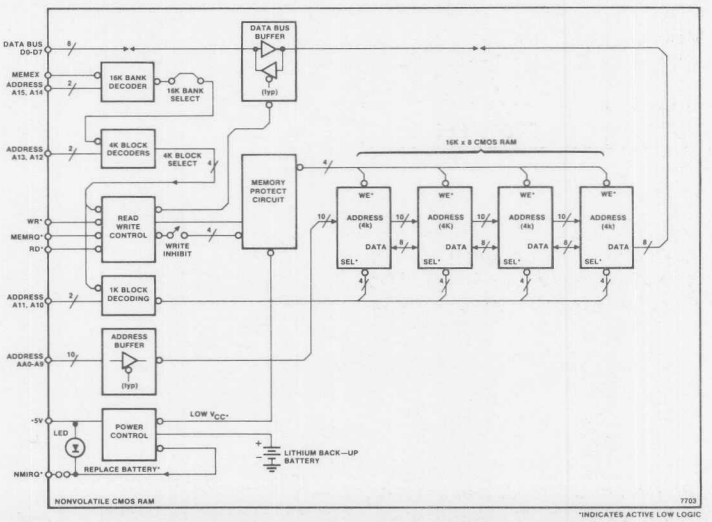
An on-board, memory-protect circuit in the 7703 monitors the +5V DC power and automatically generates a memory-save signal before switching to the lithium battery backup.

Write-protect switches (4K blocks) are available in the 7703 for preserving critical data and for nonvolatile program execution. The card decodes all 16 address lines. On-board jumpers permit mapping in any consecutive 4K, 8K, or 16K address blocks within 16K boundaries. All 7703 cards are shipped with starting address C000.



FEATURES

- **As many as 16,384 bytes of nonvolatile static CMOS RAM**
- **Available in five configurations: 1K, 2K, 4K, 8K, and 16K bytes**
- **Lithium backup battery (guaranteed to give two years of data retention, five years typical)**
- **Automatic memory protection upon loss of +5V power**
- **Transportable without loss of data**
- **Write-inhibit switches (4K blocks)**
- **Temperature range: 0 to +55°C ambient**
- **Single +5V power requirements**
- **High-speed CMOS RAMs (250ns)**
- **Full 64K address decoding**
- **Industry-standard multisourced components**
- **LED for replace-battery indication**
- **Instant operation (no battery-charging time required)**
- **Universal processor compatability—Z80, 8085, 6800, and others.**



7703, BATTERY-BACKED CMOS RAM CARD

MECHANICAL

Requires one additional open card slot next to the component side of the 7703 card, for clearance of the lithium battery when mounted in a 7000 series card rack.

STANDARD CONFIGURATIONS

The 7703 CMOS Memory Card is available in the following configurations of 250ns CMOS RAMs preinstalled and tested:

ORDER BY PRODUCT NUMBER	MEMORY SIZE	ADDRESS RANGE AS SHIPPED
7703-1C	1Kx8	C000-C3FF
7703-2C	2Kx8	C000-C7FF
7703-4C	4Kx8	C000-CFFF
7703-8C	8Kx8	C000-DFFF
7703-16C	16Kx8	C000-FFFF

Address range may be remapped by the user, within any 16K boundaries.

USER'S MANUAL

To obtain the user's manual for the 7703, ask for Pro-Log document #106293.

STD/7703 EDGE CONNECTOR PIN LIST							
PIN NUMBER	OUTPUT (DRIVE)			PIN NUMBER	OUTPUT (DRIVE)		
	INPUT (LOADING)						INPUT (LOADING)
MNEMONIC							MNEMONIC
+5V	VCC		2	1		VCC	+5V
GROUND	GND		4	3		GND	GROUND
-5V			6	5			-5V
D7	1	55	8	7	55	1	D3
D6	1	55	10	9	55	1	D2
D5	1	55	12	11	55	1	D1
D4	1	55	14	13	55	1	D0
A15	1		16	15		1	A7
A14	1		18	17		1	A6
A13	1		20	19		1	A5
A12	1		22	21		1	A4
A11	1		24	23		1	A3
A10	1		26	25		1	A2
A9	1		28	27		1	A1
A8	1		30	29		1	A0
RD*	1		32	31		1	WR*
MEMRQ*	1		34	33			IORQ*
MEMEX	1		36	35			IOEXP
MCSYNC*			38	37			REFRESH*
STATUS 0*			40	39			STATUS 1*
BUSRQ*			42	41			BUSAK*
INTRQ*			44	43			INTAK*
NMIRQ*	20 [1]		46	45			WAITRQ*
PBRESET*			48	47			SYSRESET*
CNTRL*			50	49			CLOCK*
PCI	IN		52	51	OUT		PCO
AUX GND			54	53			AUX GND
AUX -V			56	55			AUX +V

* Active low-level logic [1] Open collector driver

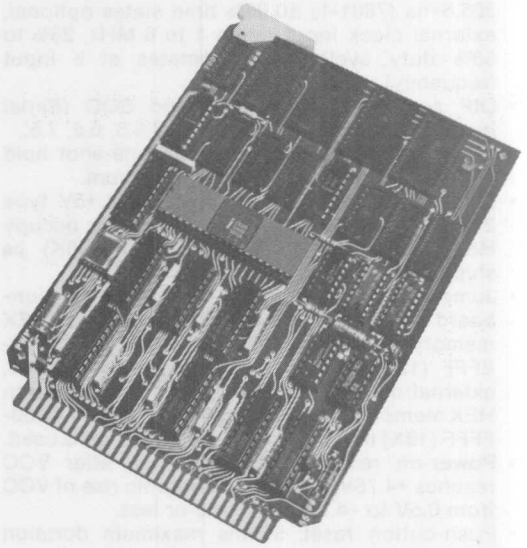
Edge Connector Pin List

7000
STD BUS

7801
8085A PROCESSOR CARD

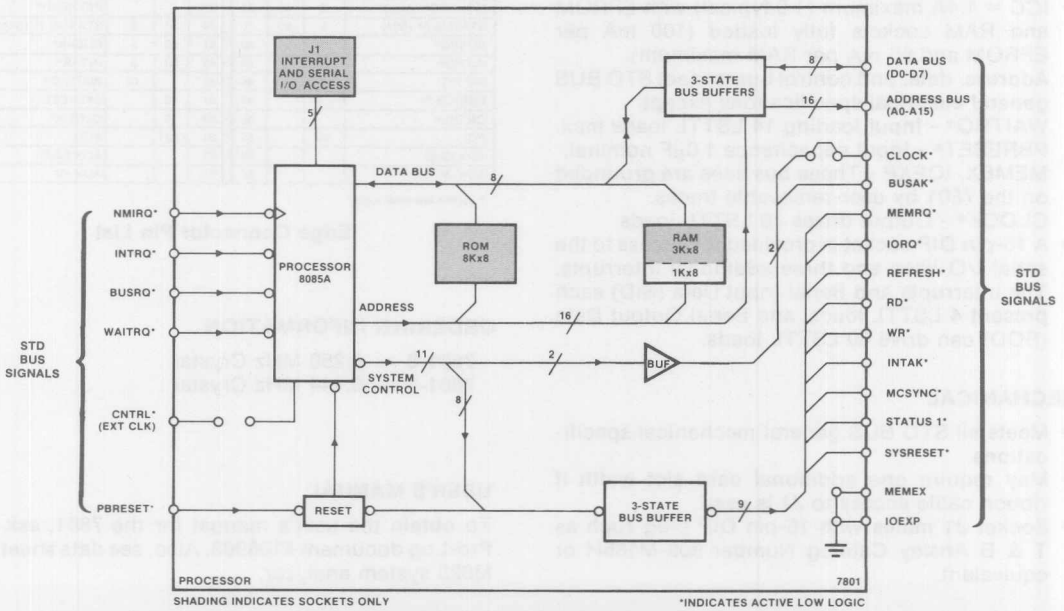
This card combines a buffered and fully expandable 8085A microprocessor with onboard RAM and PROM sockets.

The 7801 includes 1K byte of RAM with sockets for up to 4K, and sockets for up to 8K bytes of ROM or EPROM. An STD BUS system using the 7801 card can be expanded to full 8085A memory and I/O capability. The 7801 STD BUS interface may be disabled for DMA applications.



FEATURES

- **8085A Processor**
- **4096-byte RAM capacity onboard**
- **1024-byte RAM included**
- **8192-byte ROM capacity onboard**
- **3-state address, data, control buses**
- **Five hardware interrupt lines**
- **Serial I/O lines**
- **Single +5V operation**
- **Uses Pro-Log D1004 1Kx8 memories (two 2114Ls) or equivalent**
- **On-card power-on reset**
- **External push-button reset input**
- **Two Versions:**
  7801-0 with 6.250 MHz crystal (320 ns clock)
  7801-1 with 6.144 MHz crystal (325.5+ ns clock)



SHADING INDICATES SOCKETS ONLY

*INDICATES ACTIVE LOW LOGIC

7801, PROCESSOR CARD

FUNCTIONAL

- Executes all of the 8080 and 8085A processor instructions
- Crystal oscillator produces 320 ns (7801) or 325.5+ns (7801-1) ±0.05% time states optional, external clock input range 1 to 6 MHz, 25% to 50% duty cycle (card operates at ½ input frequency).
- DIP socket access to SID and SOD (Serial input/output data) and interrupts 5.5, 6.5, 7.5.
- Power-on reset and PBRESET* one-shot hold SYSRESET* active for 50 ms maximum.
- Sockets are provided for up to four +5V type 2716 EPROMs (8192 bytes total), which occupy HEX memory addresses 0000-1FFF (8K) as shipped.
- Jumper pads are provided for disabling the onboard memory or remapping it from HEX memory addresses 0000-2FFF (12K) to C000-EFFF (12K). If any onboard memory is used, external memory cards may not be mapped in HEX memory address 0000-3FFF (16K), or C000-FFFF (16K) if onboard remapping option is used.
- Power-on reset: 50 ms maximum after VCC reaches +4.75V; requires monotonic rise of VCC from 0.5V to +4.75V in 10 ms or less.
- Push-button reset: 50 ms maximum duration after release of push-button.

ELECTRICAL

- VCC = +5V ±5%
- ICC = 1.4A maximum (1.0 typical) with EPROM and RAM sockets fully loaded (100 mA per EPROM and 65 mA per RAM maximum).
- Address, data, and control buses meet STD BUS general electrical specifications except:
  WAITRQ* - Input loading 14 LSTTL loads max.
  PBRESET* - Input capacitance 1.0μF nominal.
  MEMEX, IOEXP - These bus lines are grounded on the 7801 by user-removable traces.
  CLOCK* - Output drives 10 LSTTL loads.
- A 16-pin DIP socket is provided for access to the serial I/O lines and three additional interrupts. The interrupts and Serial Input Data (SID) each present 4 LSTTL loads, and Serial Output Data (SOD) can drive 60 LSTTL loads.

MECHANICAL

- Meets all STD BUS general mechanical specifications.
- May require one additional card slot width if ribbon cable access to J1 is used.
- Socket J1 mates with 16-pin DIP plug such as T & B Ansley Catalog Number 609-M165H or equivalent.

J1 SERIAL I/O INTERRUPT PIN LIST						
PIN NUMBER	SIGNAL FLOW	SIGNAL		PIN NUMBER	SIGNAL FLOW	SIGNAL
INTR 7.5*	IN	1	16	OUT	GND
INTR 6.5*	IN	2	15	OUT	GND
INTR 5.5*	IN	3	14	OUT	GND
SOD*	OUT	4	13	OUT	GND
SID*	IN	5	12	OUT	GND
(SPARE)		6	11	OUT	GND
(SPARE)		7	10	OUT	GND
(SPARE)		8	9	OUT	GND

* Active low-level logic

J1 SERIAL I/O INTERRUPT PIN LIST

STD/7801 EDGE CONNECTOR PIN LIST							
PIN NUMBER	OUTPUT (DRIVE)	INPUT (LOADING)	MNEMONIC		PIN NUMBER	OUTPUT (DRIVE)	INPUT (LOADING)	MNEMONIC
+5V	VCC		2	1		VCC	+5V
GROUND	GND		4	3		GND	GROUND
-5V			6	5			-5V
D7	5	50	8	7	50	5	D3
D6	5	50	10	9	50	5	D2
D5	5	50	12	11	50	5	D1
D4	5	50	14	13	50	5	D0
A15	5	50	16	15	50	5	A7
A14	5	50	18	17	50	5	A6
A13	5	50	20	19	50	5	A5
A12	5	50	22	21	50	5	A4
A11	5	50	24	23	50	5	A3
A10	5	50	26	25	50	5	A2
A9	5	50	28	27	50	5	A1
A8	5	50	30	29	50	5	A0
RD*	5	50	32	31	50	5	WR*
MEMRQ*	5	50	34	33	50	5	IORQ*
MEMEX (GROUND)		OUT	36	35	OUT		IOEXP (GROUND)
MCSYNC* (ALE*)	5	50	38	37			REFRESH*
STATUS 0* (S0*)	5	50	40	39	50	5	STATUS 1* (S1*)
BUSRQ*	5		42	41	50	5	BUSAK*
INTRQ*	5		44	43	50	5	INTAK*
NMIRQ*	5		46	45		14	WAITRQ*
PBRESET*	1 μF		48	47	50		SYSRESET*
CNTRL*			50	49	10		CLOCK*
PCI	IN		52	51	OUT		PCO
AUX GND			54	53			AUX GND
AUX -V			56	55			AUX +V

* Active low-level logic

Edge Connector Pin List

ORDERING INFORMATION

7801-0 — 6.250 MHz Crystal
7801-1 — 6.144 MHz Crystal

USER'S MANUAL

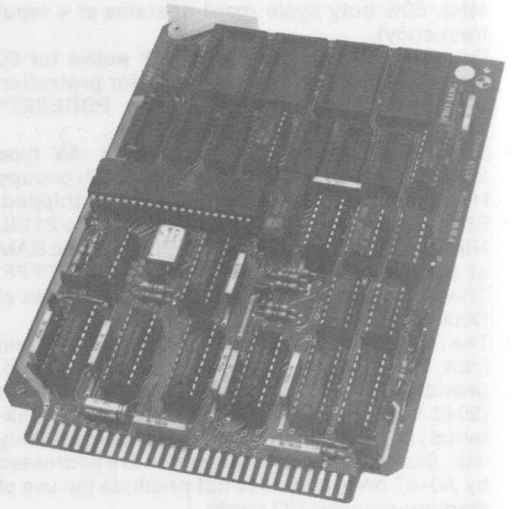
To obtain the user's manual for the 7801, ask for Pro-Log document #106903. Also, see data sheet for M825 system analyzer.

7000
STD BUS

7802
6800 PROCESSOR CARD

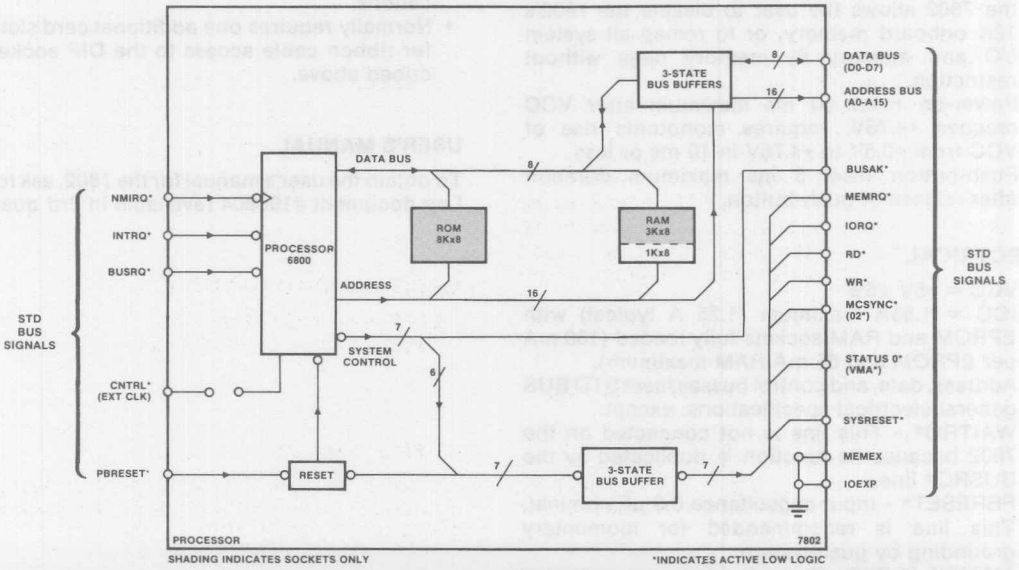
This card provides a buffered and fully expandable 6800 microprocessor with onboard RAM and PROM sockets.

The 7802 includes 1K byte of RAM with sockets for up to 4K bytes, and sockets for up to 8K bytes of ROM or EPROM. An STD BUS system using the 7802 card can be expanded to full memory and I/O capacity of the 6800. The STD BUS interface may be disabled for DMA applications.



FEATURES

- **6800 Processor**
- **4096-byte RAM capacity onboard**
- **1024-byte RAM included**
- **8192-byte ROM capacity onboard**
- **3-state address, data, control buses**
- **Crystal-controlled 1 μs clock**
- **Power-on reset and push-button reset input**
- **STD BUS compatible I/O mapping options**
- **Standard and custom memory and I/O remapping options**
- **Single +5V operation**
- **Uses Pro-Log D1004 1Kx8 memories (two 2114Ls) or equivalent**



7802, PROCESSOR CARD

FUNCTIONAL

- Executes all of the 6800 processor instructions
- Crystal oscillator produces 1.0μs ±0.05% clock cycles. External clock input range 0.4 to 4.0 MHz, 50% duty cycle (card operates at ¼ input frequency).
- Power-on reset holds SYRESET* active for 50 ms maximum. Provision is made for protection of external dynamic RAM during PBRESET* push-button reset).
- Sockets are provided for up to four +5V type 2716 EPROMs (8192 bytes total), which occupy HEX memory addresses E000-FFFF as shipped.
- Sockets are provided for up to 4K of type 2114L NMOS static RAM or type 6514 EMOS static RAM at hexadecimal memory locations D000-DFFF. The first 1K of this RAM is shipped installed at D000-D3FF.
- The 7802 generates IORQ* (I/O request) when HEX memory page address 00 is decoded, providing for 256 input and output ports each (2048 input and 2048 output lines total) on external I/O cards. This provides compatibility with Series 7000 I/O cards, which are addressed by A0-A7 only, and does not preclude the use of memory-mapped I/O cards.
- An I/O and RAM remapping jumper option is provided for the user. This option moves the I/O allocation from HEX memory page 00 to page 80, and moves RAM from HEX memory address D000-DFFF (4K) to addresses 0000-0FFF (4K). This permits either I/O or RAM to be used with the 6800's base page memory direct instructions
- Replacement of a field programmable PROM on the 7802 allows the user to disable the 7802's 12K onboard memory, or to remap all system I/O and memory by memory page without restriction.
- Power-on reset: 50 ms maximum after VCC reaches +4.75V; requires monotonic rise of VCC from +0.5V to +4.75V in 10 ms or less.
- Push-button reset: 5 ms maximum duration after release of push-button.

ELECTRICAL

- VCC = +5V ±5%
- ICC = 1.85A maximum (1.25 A typical) with EPROM and RAM sockets fully loaded (100 mA per EPROM and 65 mA RAM maximum).
- Address, data, and control busses meet STD BUS general electrical specifications, except:
  WAITRQ* - This line is not connected on the 7802 because its function is duplicated by the BUSRQ* line.
  PBRESET* - Input capacitance 0.5 μF nominal. This line is recommended for momentary grounding by push-button.
  MEMEX, IOEXP - These bus lines are grounded on the 7802 by user-removable jumper traces.

STD/7802 EDGE CONNECTOR PIN LIST							
PIN NUMBER				PIN NUMBER			
OUTPUT (DRIVE)					OUTPUT (DRIVE)		
INPUT (LOADING)						INPUT (LOADING)	
MNEMONIC							MNEMONIC
+5V	VCC		2	1		VCC	+5V
GROUND	IN		4	3		IN	GROUND
-5V			6	5			-5V
D7	5	50	8	7	50	5	D3
D6	5	50	10	9	50	5	D2
D5	5	50	12	11	50	5	D1
D4	5	50	14	13	50	5	D0
A15	5	50	16	15	50	5	A7
A14	5	50	18	17	50	5	A6
A13	5	50	20	19	50	5	A5
A12	5	50	22	21	50	5	A4
A11	5	50	24	23	50	5	A3
A10	5	50	26	25	50	5	A2
A9	5	50	28	27	50	5	A1
A8	5	50	30	29	50	5	A0
RD*	5	50	32	31	50	5	WR*
MEMRQ*	5	50	34	33	50	5	IORQ*
MEMEX (GROUND)		OUT	36	35	OUT		IOEXP (GROUND)
MCSYNC* (02*)	5	50	38	37	50		REFRESH* (DRIVER)
STATUS 0* (VMA*)	5	50	40	39			STATUS 1*
BUSRQ*	5		42	41	50	5	BUSAK*
INTRQ*	5		44	43			INTAK*
NMIRQ*	5		46	45			WAITRQ*
PBRESET*	0.5μF		48	47	50	5	SYSRESET*
CNTRL* (EXT CLK)	[1]		50	49			CLOCK*
PCI	IN		52	51	OUT		PCO
AUX GND			54	53			AUX GND
AUX -V			56	55			AUX +V

* Active low-level logic [1] User optional connection

Edge Connector Pin List

MECHANICAL

- Meets all STD BUS general mechanical specifications.
- Normally requires one additional card slot width for ribbon cable access to the DIP socket described above.

USER'S MANUAL

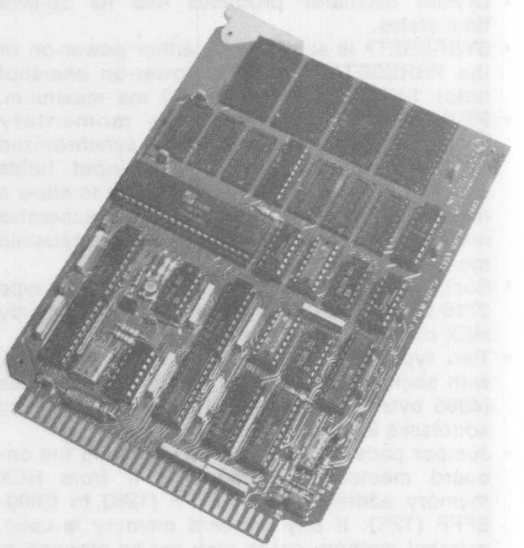
To obtain the user's manual for the 7802, ask for Pro-Log document #106904 (available in 3rd quarter).

7000 STD BUS

7803 Z80 PROCESSOR CARD

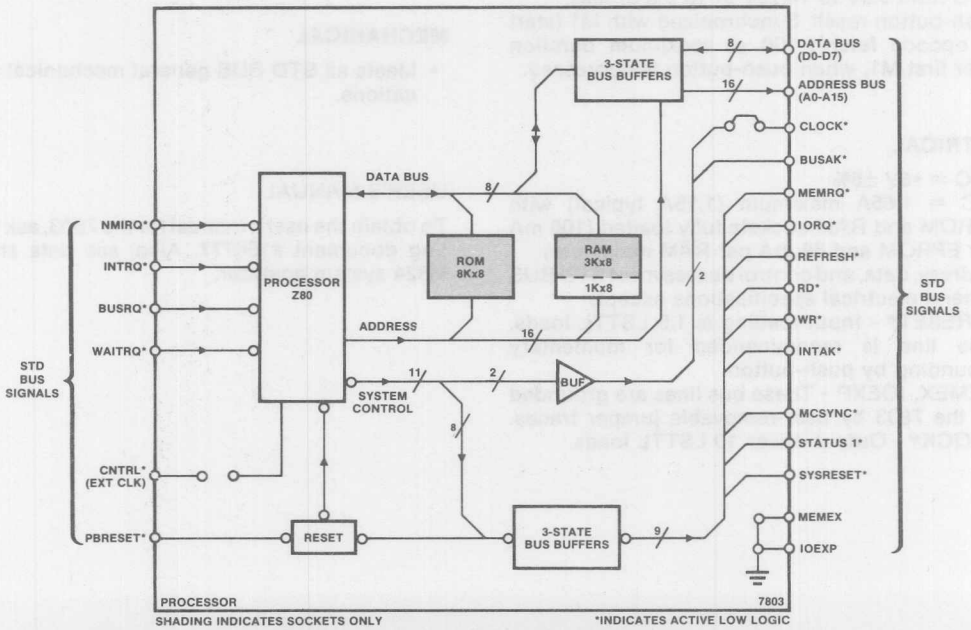
This card combines a buffered and fully expandable Z80 microprocessor with onboard RAM and PROM sockets.

The 7803 includes 1K byte of RAM with sockets for up to 4K bytes, and sockets for up to 8K bytes of ROM or EPROM. An STD BUS system using the 7803 card can be expanded to full Z80 memory and I/O capability. The 7803 STD BUS interface may be disabled for DMA applications.



FEATURES

- **Z80 Processor**
- **4096-byte RAM capacity (type 2114)**
- **1024-byte RAM included**
- **8192-byte ROM capacity onboard (type 2716 EPROM)**
- **3-state address, data, control buses**
- **Crystal-controlled 400 ns clock**
- **Dynamic RAM refresh control**
- **Single +5V operation**
- **Uses Pro-Log D1004 1Kx8 memories (two 2114Ls) or equivalent**
- **On-card power-on reset (with defeatable refresh sync)**
- **External push-button reset input**



7803, PROCESSOR CARD

FUNCTIONAL

- Executes all of the 8080 and Z80 processor instructions.
- Crystal oscillator produces 400 ns ±0.05% time states.
- SYSRESET* is activated by either power-on or the PBRESET* input. The power-on one-shot holds SYSRESET* low for 50 ms maximum.
- PBRESET* is intended for momentary grounding by push-button and is synchronized to the processor timing. This input holds SYSRESET* low for 10 μs maximum to allow a manual processor reset without excessive interruption of the REFRESH* output to dynamic memories.
- Sockets are provided for up to four +5V type 2716 EPROMs (8192 bytes total), which occupy HEX memory addresses 0000-1FFF (8K).
- Two type 2114 RAMs (1024 bytes) included, with sockets for up to eight total RAM devices (4096 bytes total), which occupy HEX memory addresses 2000-2FFF (4K).
- Jumper pads are provided for disabling the onboard memory or remapping it from HEX memory addresses 0000-2FFF (12K) to C000-EFFF (12K). If any onboard memory is used, external memory cards may not be mapped in HEX memory address 0000-3FFF (16K), or C000-FFFF (16K) if onboard remapping option is used.
- Power-on reset: 150 ms maximum after VCC reaches +4.75V; requires monotonic rise of VCC from 0.5V to +4.75V in 10 ms or less.
- Push-button reset: Synchronized with M1 (start of opcode fetch); 100 μs maximum duration after first M1, when push-button is depressed.

ELECTRICAL

- VCC = +5V ±5%
  ICC = 1.65A maximum (1.15A typical) with EPROM and RAM sockets fully loaded (100 mA per EPROM and 65 mA per RAM maximum).
- Address, data, and control busses meet STD BUS general electrical specifications except:
  PBRESET* - Input loading is 1.5 LSTTL loads. This line is recommended for momentary grounding by push-button.
  MEMEX, IOEXP - These bus lines are grounded on the 7803 by user-removable jumper traces.
  CLOCK* - Output drives 10 LSTTL loads.

STD/7803 EDGE CONNECTOR PIN LIST							
PIN NUMBER	OUTPUT (DRIVE)	INPUT (LOADING)	MNEMONIC	PIN NUMBER	OUTPUT (DRIVE)	INPUT (LOADING)	MNEMONIC
+5V	VCC		2	1		VCC	+5V
GROUND	IN		4	3		IN	GROUND
-5V			6	5			-5V
D7	5	50	8	7	50	5	D3
D6	5	50	10	9	50	5	D2
D5	5	50	12	11	50	5	D1
D4	5	50	14	13	50	5	D0
A15	5	50	16	15	50	5	A7
A14	5	50	18	17	50	5	A6
A13	5	50	20	19	50	5	A5
A12	5	50	22	21	50	5	A4
A11	5	50	24	23	50	5	A3
A10	5	50	26	25	50	5	A2
A9	5	50	28	27	50	5	A1
A8	5	50	30	29	50	5	A0
RD*	5	50	32	31	50	5	WR*
MEMRQ*	5	50	34	33	50	5	IORQ*
MEMEX (GROUND)		OUT	36	35	OUT		IOEXP (GROUND)
MCSYNC* (RD*-WR8-INTA*)	5	50	38	37	50	5	REFRESH*
STATUS 0*	5	50	40	39	50	5	STATUS 1* (M2*)
BUSRQ*	5		42	41	50	5	BUSAK*
INTRQ*	5		44	43	50	5	INTAK*
NMIRQ*	5		46	45		5	WAITRQ*
PBRESET*	15		48	47	50	5	SYSRESET*
CNTRL*			50	49	10	5	CLOCK*
PCI	IN		52	51	OUT		PCO
AUX GND			54	53			AUX GND
AUX -V			56	55			AUX +V

* Active low-level logic

Edge Connector Pin List

MECHANICAL

- Meets all STD BUS general mechanical specifications.

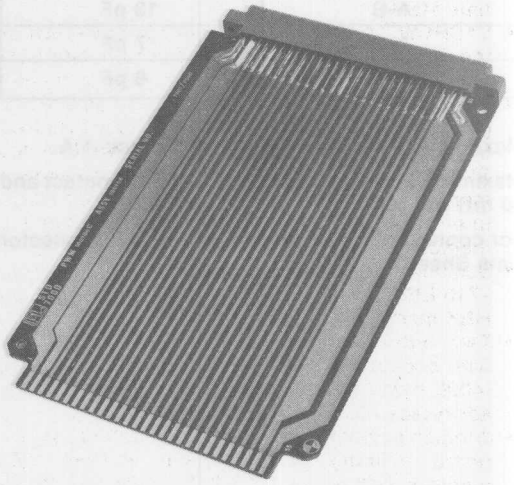
USER'S MANUAL

To obtain the user's manual for the 7803, ask for Pro-Log document #106777. Also, see data sheet for M824 system analyzer.

7000 STD BUS

7901 UTILITY CARD EXTENDER

The 7901 is a printed circuit card for extending cards out of the card cage for easy access. The 7901 (8411, P560) card extender can be used with all Pro-Log edge connected cards.

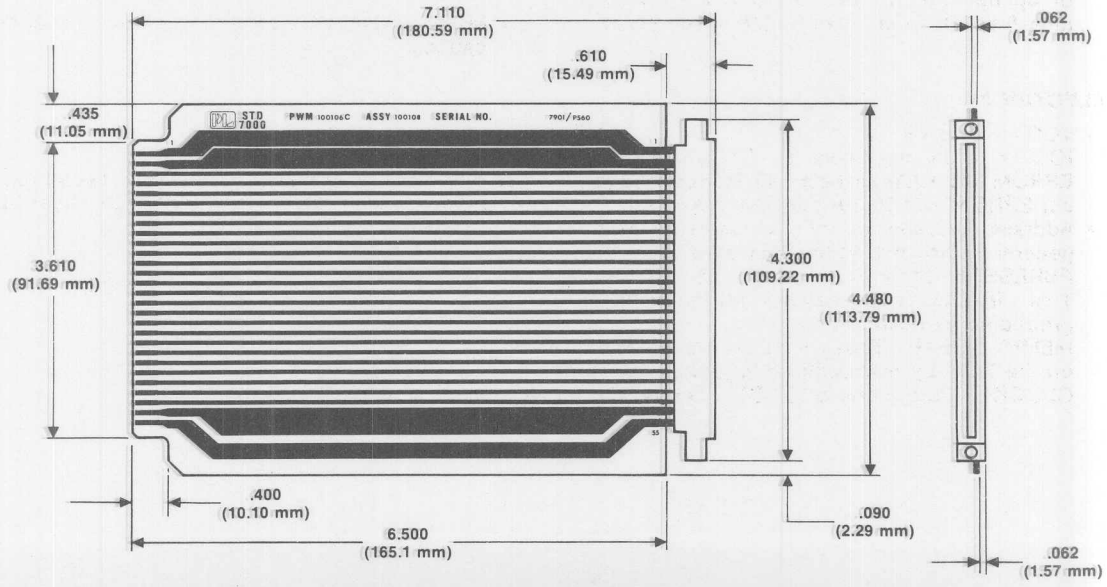


CARD DIMENSIONS

- 4.48 in. (113.79 mm) high by 7.11 in. (180.59 mm) long
- 0.062 in. (1.58 mm) printed circuit board thickness

CONNECTOR REQUIREMENTS

56-pin, 28-position, dual readout on 0.125 in. (3.18 mm) pin centers. See CW56, CW56-1 Edge Card Connector Data Sheet.



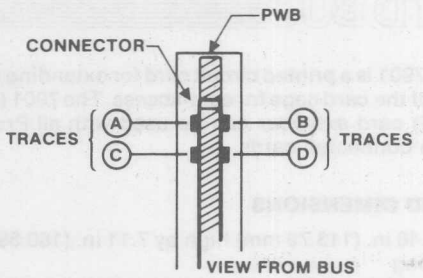
7901, UTILITY CARD EXTENDER

MAX TRACE-TO-TRACE CAPACITANCE INCLUDING THE CONNECTOR	
A-B	13 pF
A-C	7 pF
A-D	6 pF

Maximum current per trace and contact: 1 A.

Maximum insertion resistance: 10 mΩ/contact and 60 mΩ per trace.

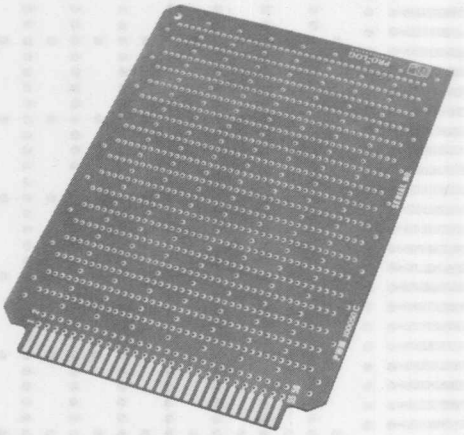
For connector specifications, see CW56 Connector Data Sheet.



STD BUS Card Edge Connector Configuration

7902
UTILITY DIP CARD

The 7902 is a printed circuit card for prototyping with dual-in-line (DIP) packaging. It accommodates 8, 14, 16, and 18 pin DIPs on 0.300 in. (7.62 mm) centers and 24, 28, and 40-pin DIPs on 0.600 in. (15.24 mm) centers. Card has printed power distribution bus. Plated-through holes accommodate 0.025 in. (0.64 mm) square posts for wrapped wire connection.



CARD DIMENSIONS

- 4.48 in. (113.79 mm) high by 6.5 in. (165.1 mm) long
- 0.062 in. (1.58 mm) printed circuit board thickness
- 0.035 in. (0.89 mm) diameter plated-through holes

CONNECTOR REQUIREMENTS

56-pin, 28-position, dual readout on 0.125 in. (3.18 mm) pin centers. See CW56, CW56-1 Edge Card Connector Data Sheet.

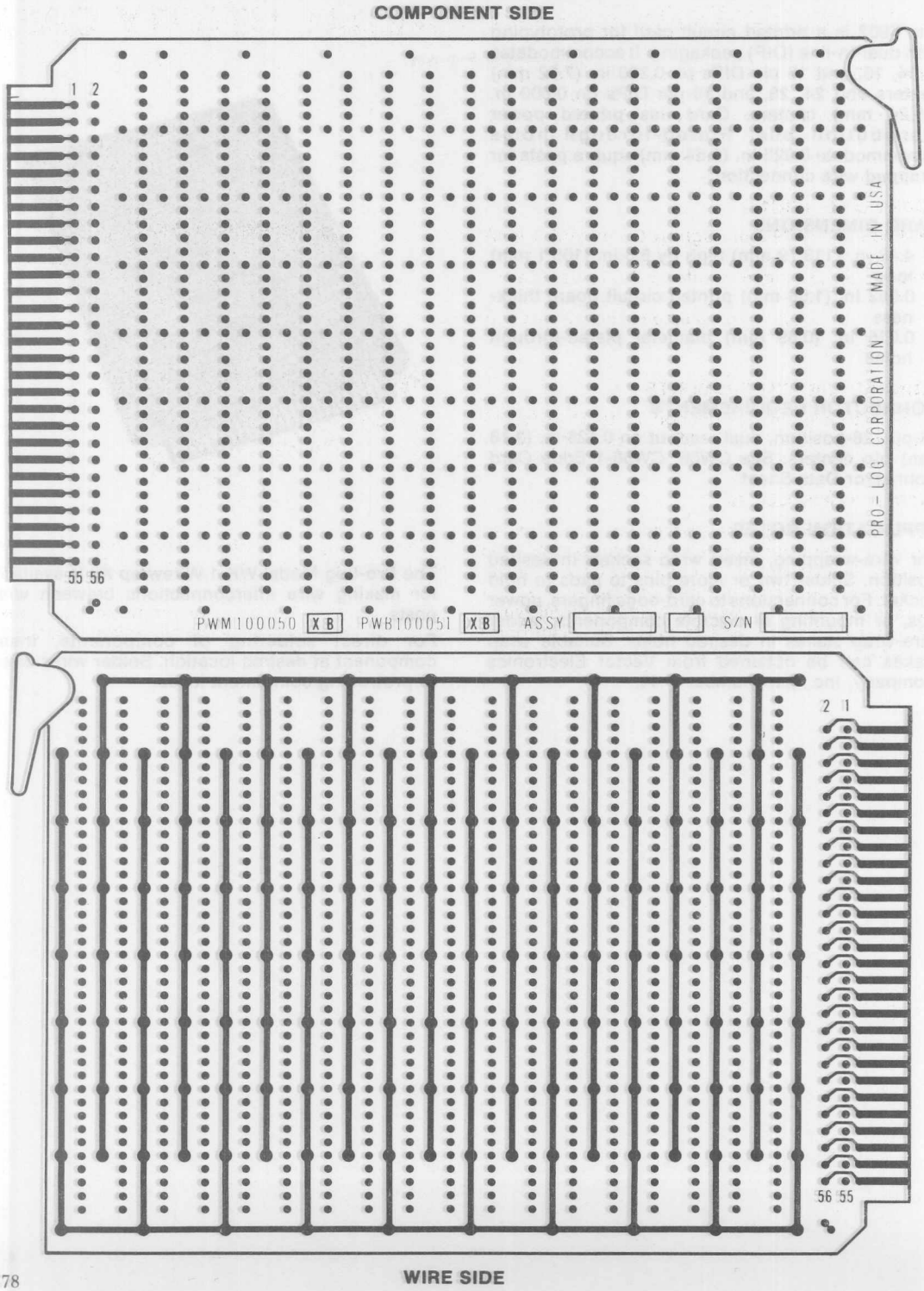
APPLICATION NOTES

For wire-wrapping, insert wrap sockets in desired position. Solder two or more pins to pads to hold socket. For connections to card-edge fingers, power bus, or mounting of discrete components, solder wire-wrap stakes in desired holes. Suitable wrap stakes can be obtained from Vector Electronics Company, Inc., part number T-44.

The Pro-Log Model WK-1 Wirewrap Kit is available for making wire interconnections between wrap posts.

For direct soldering of components, insert component at desired location. Solder wires direct to protruding component leads.

7902, UTILITY DIP CARD



7000 STD BUS

7903 GENERAL UTILITY CARD

The 7903 is a printed circuit card for prototyping with 0.100 in. (2.5 mm) grid hole pattern. It accommodates discrete components or dual-in-line (DIP) packaging. Plated-through holes accommodate 0.025 in. (0.64 mm) square posts for wrapped wire connections.

CARD DIMENSIONS

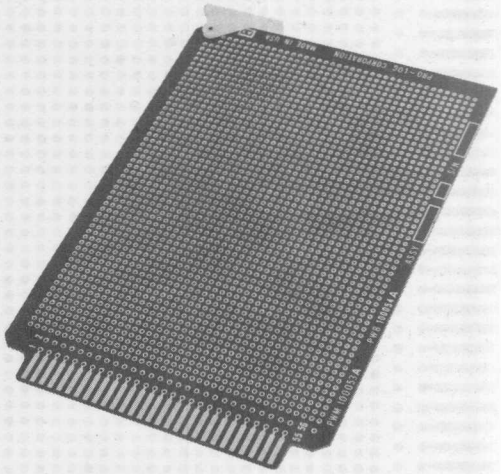
- 4.48 in. (113.79 mm) high by 6.5 in. (165.1 mm) long
- 0.062 in. (1.58 mm) printed circuit board thickness
- 0.035 in. (0.89 mm) diameter plated-through holes

CONNECTOR REQUIREMENTS

56-pin, 28-position, dual readout on 0.125 in. (3.185 mm) pin centers. See CW56, CW56-1 Edge Card Connector Data Sheet.

APPLICATION NOTES

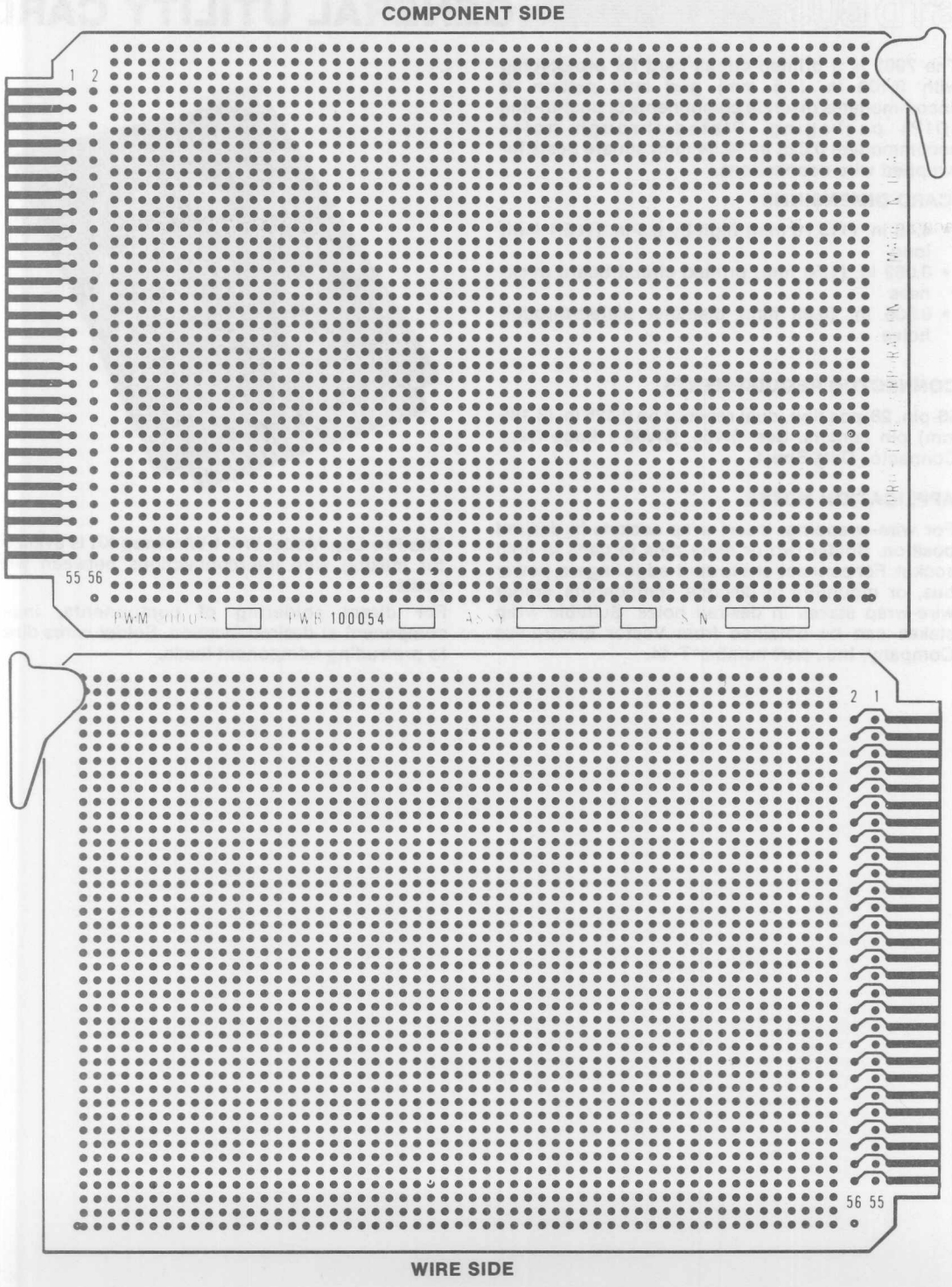
For wire-wrapping, insert wrap sockets in desired position. Solder two or more pins to pads to hold socket. For connections to card-edge fingers, power bus, or mounting of discrete components, solder wire-wrap stakes in desired holes. Suitable wrap stakes can be obtained from Vector Electronics Company, Inc., part number T-44.



The Pro-Log Model WK-1 Wirewrap Kit is available for making wire interconnections between wrap posts.

For direct soldering of components, insert component at desired location. Solder wires direct to protruding component leads.

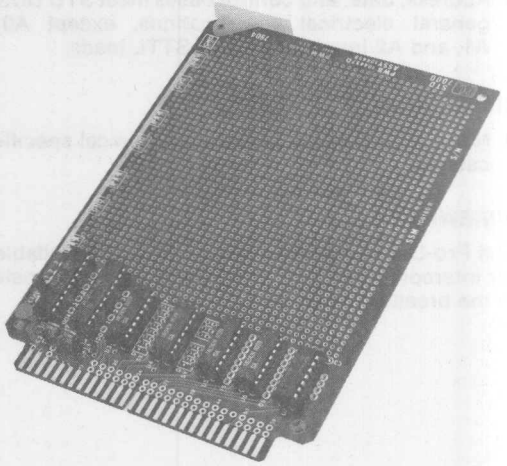
7903, GENERAL UTILITY CARD



7000 STD BUS

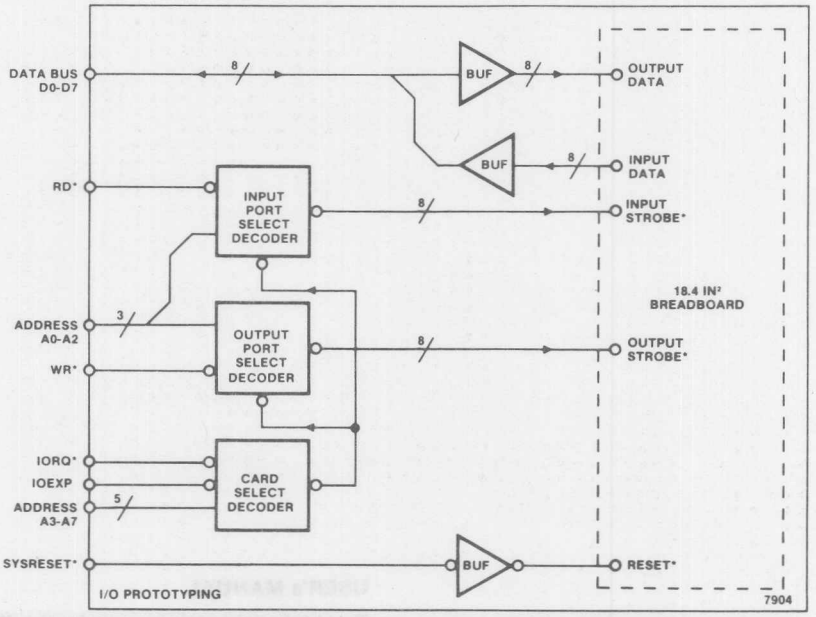
7904 DECODED I/O UTILITY CARD

The 7904 is a printed circuit card for prototyping I/O circuitry. It provides complete STD BUS buffering and decoding for I/O cards, with input and output port strobe logic and access to memory page and CPU/memory control lines. A 4x6 in. (101.6x114.6 mm) grid of holes on 0.1 in. (2.54 mm) centers is provided for adding dual-in-line or discrete packages. These plated-through holes accommodate 0.025 in. (0.64 mm) square wirewrap posts.



FEATURES

- **User-selectable port address (256-port field)**
- **Data bus buffers with hysteresis**
- **8 sequentially addressed input port strobes**
- **8 sequentially addressed output port strobes**
- **Access to all STD BUS signals and power buses**
- **LSTTL logic**
- **Plated-through holes accommodate 0.025 in. (0.64 mm) square post**
- **18.4 sq. in (118.74 cm²) of breadboard area**
- **Universal processor compatibility—Z80, 8085, 6800, and others.**



*INDICATES ACTIVE LOW LOGIC

7904, DECODED I/O UTILITY CARD

ELECTRICAL

- VCC = +5V ±5%
- ICC = 170 mA maximum (100 mA typical) for logic provided
- Address, data, and control buses meet STD BUS general electrical specifications, except A0, A1, and A2 inupt loading 2 LSTTL loads.

MECHANICAL

- Meets all STD BUS general mechanical specifications.

WIREWRAP KIT

The Pro-Log Model WK-1 Wirewrap Kit is available for interconnect wiring when using wirewrap posts in the breadboard area.

STD/7904 EDGE CONNECTOR PIN LIST							
PIN NUMBER	OUTPUT (DRIVE)	INPUT (LOADING)	MNEMONIC	PIN NUMBER	OUTPUT (DRIVE)	INPUT (LOADING)	MNEMONIC
+5V	VCC		2	1		VCC	+5V
GROUND	IN		4	3		IN	GROUND
-5V			6	5			-5V
D7	1	55	8	7	55	1	D3
D6	1	55	10	9	55	1	D2
D5	1	55	12	11	55	1	D1
D4	1	55	14	13	55	1	D0
A15			16	15		1	A7
A14			18	17		1	A6
A13			20	19		1	A5
A12			22	21		1	A4
A11			24	23		1	A3
A10			26	25		2	A2
A9			28	27		2	A1
A8			30	29		2	A0
RD*	1		32	31		1	WR*
MEMRQ*			34	33		1	IORQ*
MEMEX			36	35		1	IOEXP
MCSYNC*			38	37			REFRESH*
STATUS 0*			40	39			STATUS 1*
BUSRQ*			42	41			BUSAK*
INTRQ*			44	43			INTAK*
NMIRQ*			46	45			WAITRQ*
PBRESET*			48	47		1	SYSRESET*
CNTRL*			50	49			CLOCK*
PCI	IN		52	51	OUT		PCO
AUX GND			54	53			AUX GND
AUX -V			56	55			AUX +V

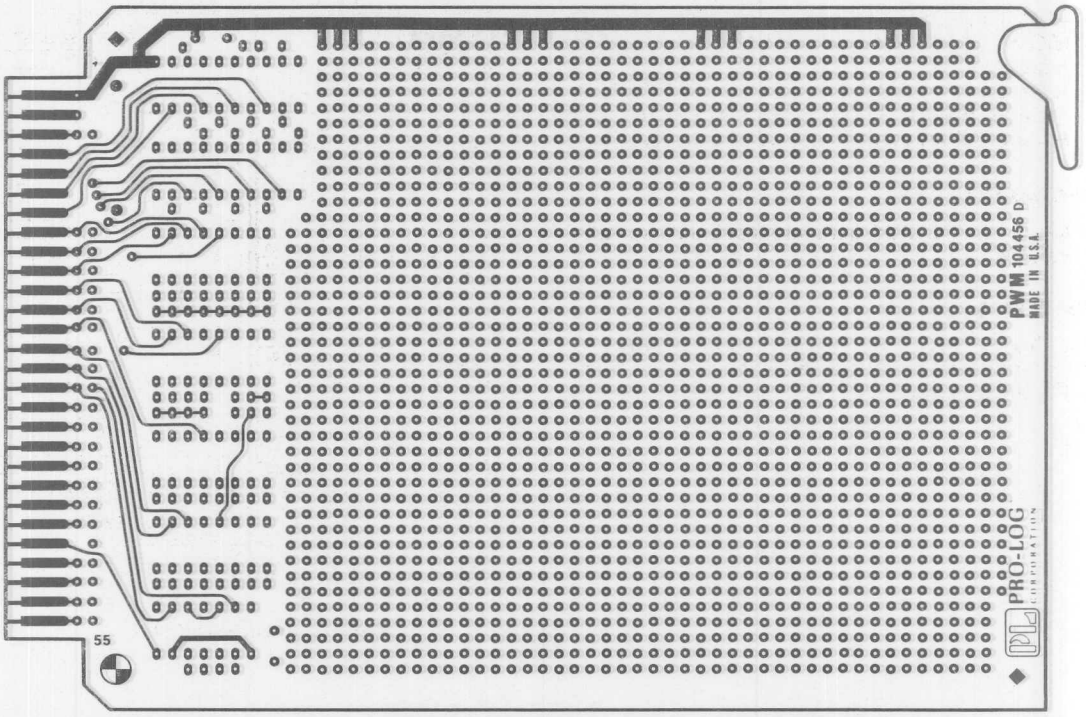
* Active low-level logic

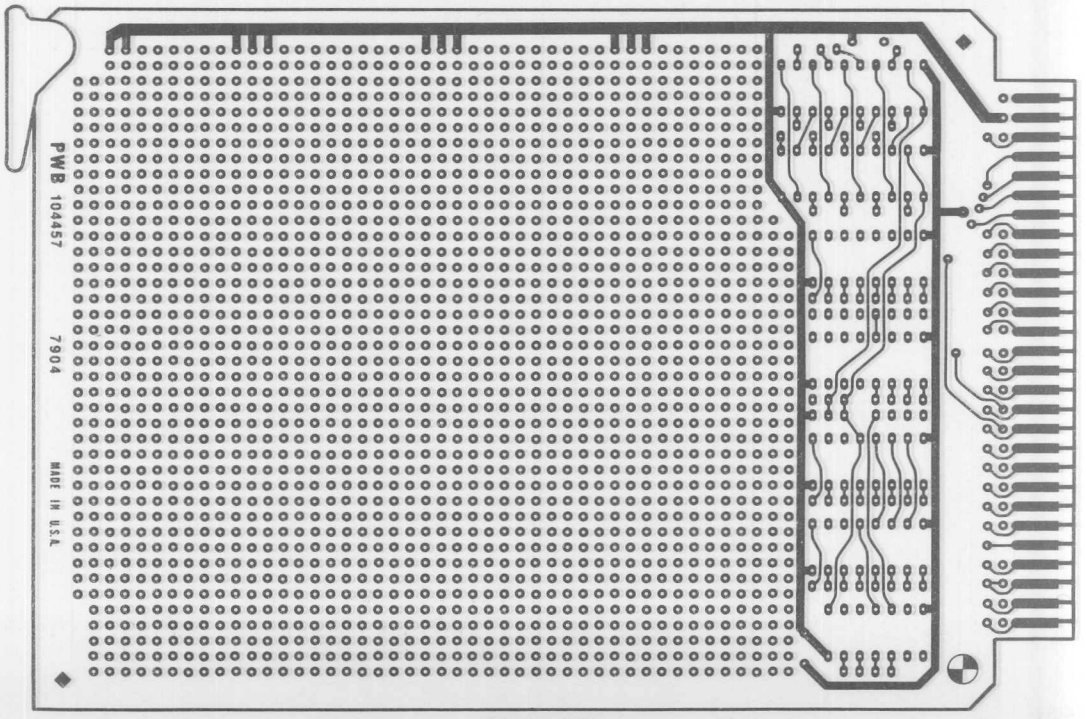
Edge Connector Pin List

USER's MANUAL

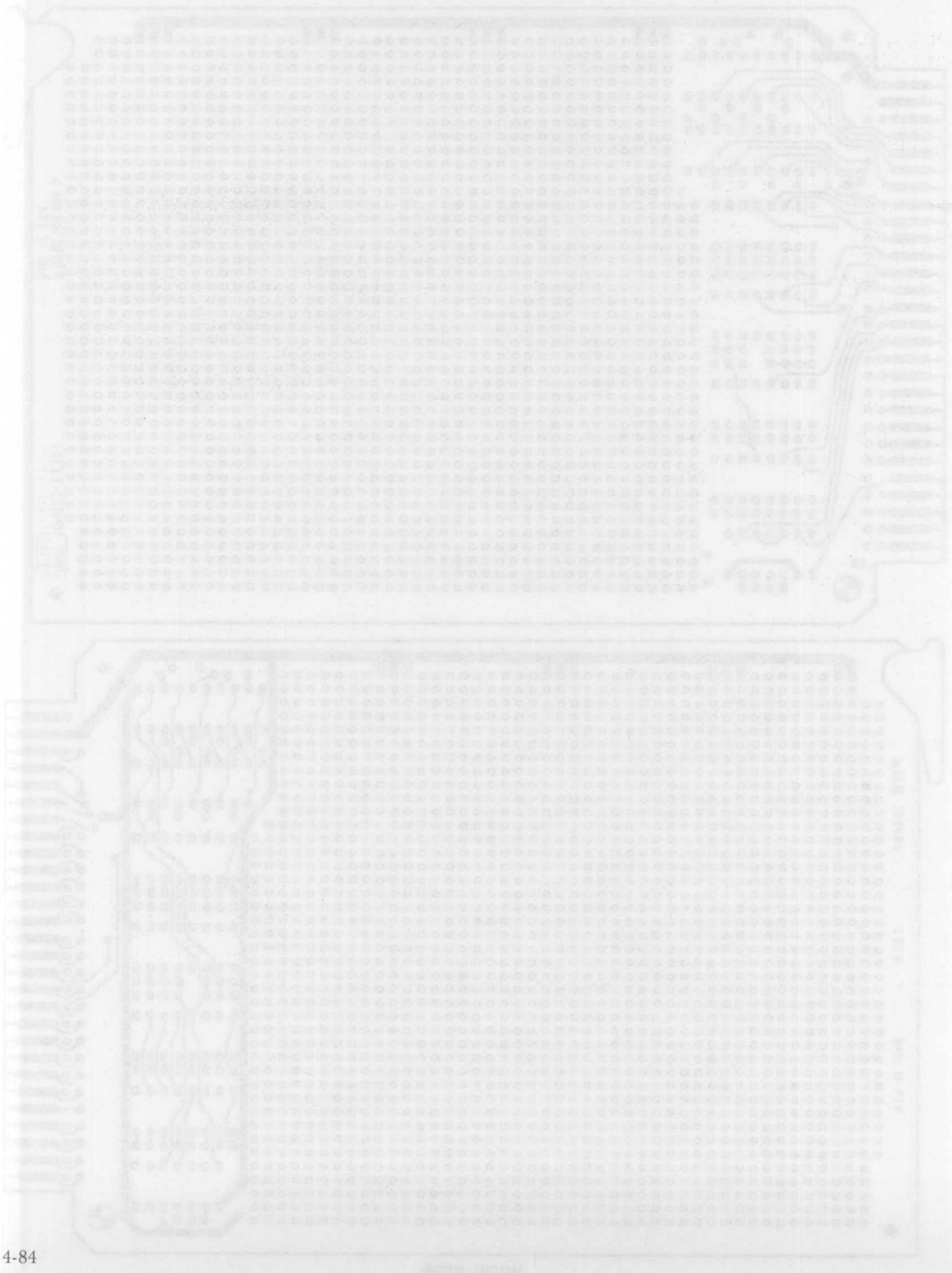
To obtain the user's manual for the 7904, ask for Pro-Log document #106406.

COMPONENT SIDE





WIRE SIDE



7000 STD BUS

7920/7921 IN-RACK POWER SUPPLIES

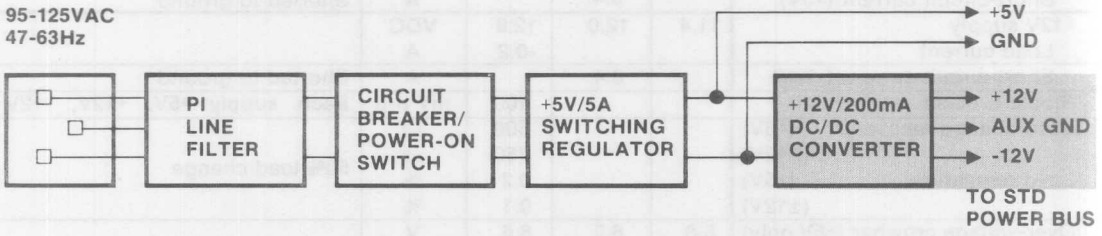
7920 SINGLE IN-RACK POWER SUPPLY, +5V
7921 TRIPLE IN-RACK POWER SUPPLY, +5V, ±12V

The 7920 is a complete +5V/5A power supply with AC line cord, line switch with LED indicator, and magnetic circuit breaker assembled on an STD BUS-compatible circuit card. The card features a low-profile, encapsulated power supply module that uses switching techniques for high efficiency and low operating temperature. The 7920's output drives the STD Logic Power Bus (+5V and logic ground).

The 7921 provides +5V at 3A minimum to the logic bus and a ±12V supply to the STD auxiliary power bus (aux +V, aux -V, aux gnd). The ±12V supplies provide 200mA each and are powered by the +5V supply.

FEATURES

- **Low profile, two card slots (card slot on far right)**
- **Single output +5V/5A (7920)**
- **Triple output +5V/3A minimum and ±12V/0.2A each (7921)**
- **Complete AC line operation on 4.5 x 6.5 in. (114.3x165.1 mm) card**
- **Power switch with LED indicator and circuit breaker**
- **Short circuit protected outputs**
- **95-125VAC, 47-63Hz operation**
- **AC line filter with separate plug-in power cord**
- **Six-sided RFI shielding**



7920 (excludes shaded area)
7921 (includes shaded area)

7920/7921 IN-RACK POWER SUPPLIES

FUNCTIONAL

The 7920 is a compact, line-operated, switching power supply that produces 5VDC at 5A with 80% efficiency. The output has both short-circuit protection and over-voltage protection, with the crowbar fixed at 6.5V. Line power is supplied via an IEC connector/filter, and the 7920 circuitry is protected with a circuit breaker.

The 7921 power supply is identical to the 7920, with the exception of an additional DC-DC converter that operates from the +5V supply to provide ±12VDC outputs at 0.2A each. When the DC-DC converter is operating under full load, the maximum +5VDC supply current available is 3A.

ELECTRICAL

PARAMETER (0°C to +40°C)①	MIN	TYP	MAX	UNIT	COMMENT
AC INPUT					
Voltage	95	115	125	VAC	Sine wave operation only
Frequency	47	50/60	63	Hz	
Power		32		W	7920 full load
		7		W	7920 no load
		32		W	7921 full load
		10		W	7921 no load
DC OUTPUTS — 7920 only					
+5V supply	4.65	5.00	5.15	VDC	
Available load current	5.0			A	
Short-circuit current		6.3		A	
Load regulation			0.2	%	50% load change
Load change recovery			500	µs	
Efficiency	75	80		%	
Ripple & Noise			100	mV p-p	DC to 20mHz measurement range
Over-voltage crowbar	5.8	6.0	6.6	V	
DC OUTPUTS — 7921 only					
+5V Supply	4.65	5.00	5.15	VDC	
Available load current②	3.0		4.5	A	Varies with ±12V load
Short-circuit current (+12V)		6.3		A	Shorted to ground
-12V supply	11.4	12.0	12.6	VDC	
Load current			0.2	A	
Short-circuit current (+5V)		0.4		A	Shorted to ground
+12V supply	11.4	12.0	12.6	VDC	
Load current			-0.2	A	
Short-circuit current (-12V)		0.4		A	Shorted to ground
Ripple & noise			100	mV p-p	Each supply: +5V, +12V, -12V
Load change recovery (+5V)			500	µs	50% load change
(±12V)			750	µs	
Load regulation (+5V)			0.2	%	
(±12V)			0.1	%	
Over-voltage crowbar (+5V only)	5.8	6.0	6.6	V	
Risetime (+5V)③		10		ms	
(±12V)		100		ms	

①Derate outputs 2% per °C to +55°C.

②Minimum current available from the +5V supply under any rated conditions is 3A. Maximum +5V current with the ±12V supplies unloaded is 4.5A. The output current available from the +5V supply decreases approximately 3.5mA for each 1Ma supplied by the ±12V supplies.

③May not provide power-on reset for some microprocessors; manual reset may be required.

MECHANICAL

The 7920 and 7921 power supplies are designed for operation in the far right card slot of Pro-Log's injection-molded card racks (CR4A, CR8A, and CR16A). Mounting in this position allows for the removal of heat from the rack, and the 7920 or 7921 card will occupy only two card slots. If mounted in any other position in the rack, the 7920 or 7921 card will occupy 4 card slots and cause the air temperature within the rack to increase.

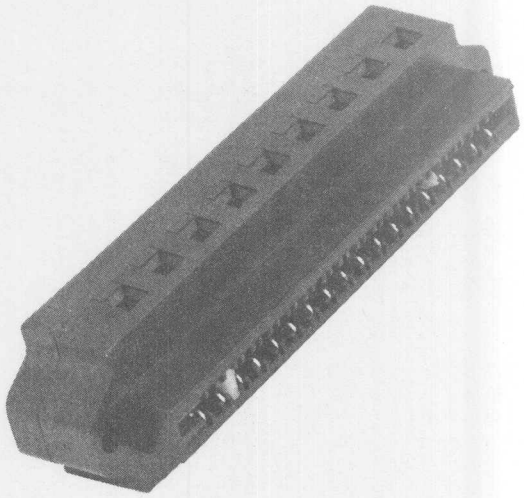
	EDGE CONNECTOR PIN LIST						
	PIN NUMBER / SIGNAL FLOW / MNEMONIC			PIN NUMBER / SIGNAL FLOW / MNEMONIC			
	+5V	OUT	2	1	OUT	+5V	
	LOGIC GROUND	OUT	4	3	OUT	LOGIC GROUND	
			6	5			
			8	7			
			10	9			
			12	11			
			14	13			
			16	15			
			18	17			
			20	19			
			22	21			
			24	23			
			26	25			
			28	27			
			30	29			
			32	31			
			34	33			
			36	35			
			38	37			
			40	39			
			42	41			
			44	43			
			46	45			
			48	47			
			50	49			
			52	51			
7921 ONLY	AUX GND	OUT	54	53	OUT	AUX GND	7921 ONLY
	-12V	OUT	56	55	OUT	+12V	

7920/7921 In-Rack Power Supplies

CB18 I/O EDGE CONNECTOR

BARRIER STRIP CONNECTOR

The CB18 card edge connector is used on industrial interface cards requiring more than 50VDC and/or 0.5A per contact.

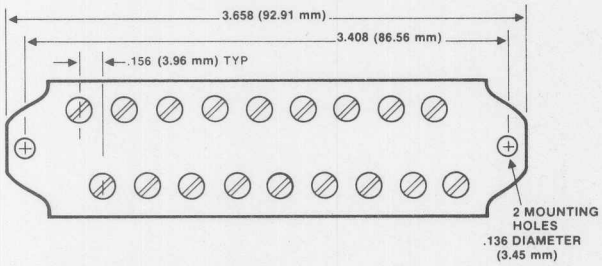


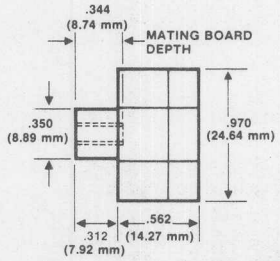
FEATURES

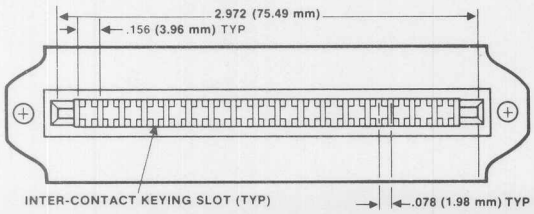
- **10A maximum per-contact**
- **Single sourced**
- **Accepts PCBs of 0.062 in. (1.57 mm) thickness**
- **Tubular contact plate accepts #12 to #22 AWG wires**
- **Includes keys**
- **UL listed**

ELECTRICAL

- Material UL rated 94V-0 (flame rating)
- Contact spacing: 0.156 in. (3.96 mm) centers
- Contact rating: 10A/circuit continuous
- Breakdown voltage: 2500V
- Operating temperature: -55°C to +105°C at sea level
- PCB thickness: 0.054 to 0.071 in. (1.37 to 1.80 mm)
- Not recommended for more than 20 insertion/withdrawals.







CONNECTOR ORDERING INFORMATION

The part numbers for the various connector manufacturers are given below.

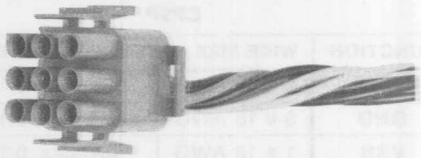
Pro-Log	CB18*
Buchanan	PCB2B Connector PC17 Keying plug

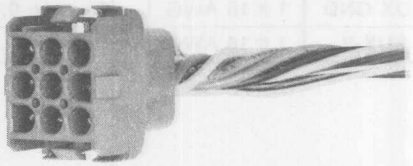
* Includes two keying plugs

7000 STD BUS

CP9P/CP9S POWER SUPPLY CONNECTOR ASSEMBLIES

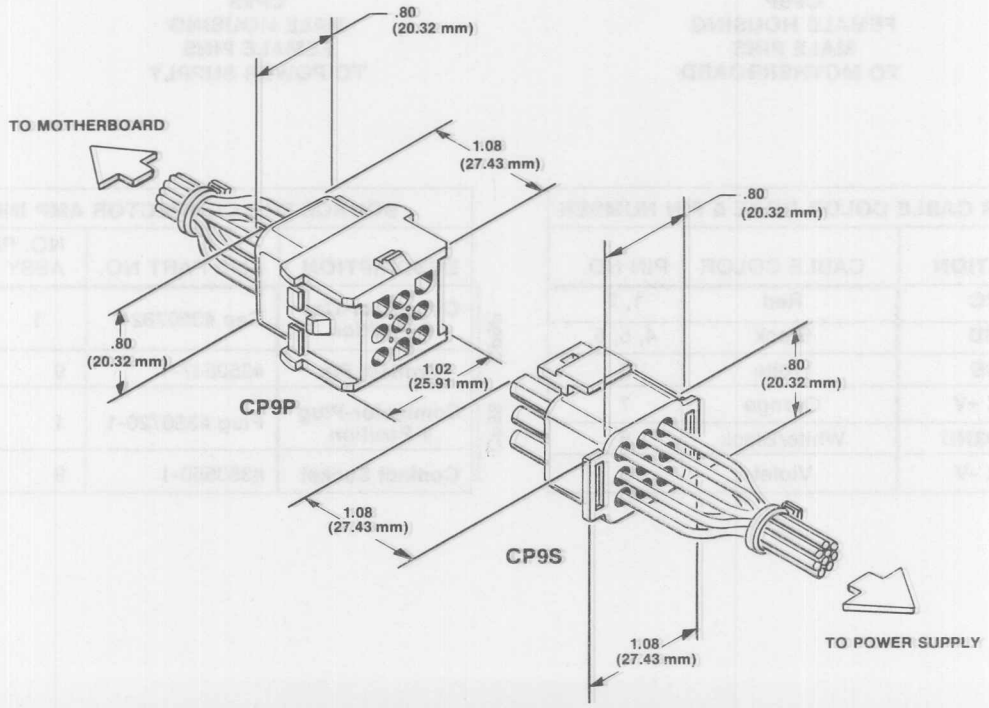
The CP9P/CP9S connector assemblies are used with Pro-Log's 7100 Series Motherboards, CR Series STD BUS Card Racks, and the M280/M281 Power Supplies. The CP9S mating socket includes a 12 in. (304.8 mm) cable with nine 16-gauge wires that connect to the power supply. The CP9P consists of a 9-pin plug and 12 in. (304.8 mm) cable with nine, 18-gauge wires that connect to the motherboard or card rack. These connectors are UL listed and feature high current contacts with recessed, protected pins and low force, polarized and locking housing.





FEATURES

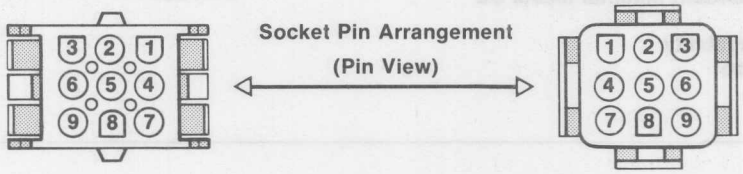
- **Used for the Series 7000 power interconnect**
- **UL listed**
- **Interlocking design with protected pins**
- **Supplies all STD BUS backplane power**
- **90-VO flame-retardant material meets UL standard 1410**
- **High-current capability**
- **Low-voltage drop**



CP9P/CP9S POWER SUPPLY CONNECTOR ASSEMBLIES

POWER INTERCONNECT CABLE

POWER CABLE AND CONNECTOR SPECIFICATIONS					
CP9P			CP9S		
FUNCTION	WIRE SIZE	RECOMMENDED LOAD	FUNCTION	WIRE SIZE	RECOMMENDED LOAD
VCC	2 # 18 AWG	12A max, 0.1A min	VCC	2 # 16 AWG	20A max, 0.1A min
GND	3 # 18 AWG	12A max, 0.1A min	GND	3 # 16 AWG	20A max, 0.1A min
VBB	1 # 18 AWG	6A max, 0.1A min	VBB	1 # 16 AWG	10A max, 0.1A min
AUX+V	1 # 18 AWG	6A max, 0.1A min	AUX+V	1 # 16 AWG	10A max, 0.1A min
AUX GND	1 # 18 AWG	6A max, 0.1A min	AUX GND	1 # 16 AWG	10A max, 0.1A min
AUX-V	1 # 18 AWG	6A max, 0.1A min	AUX-V	1 # 16 AWG	10A max, 0.1A min



CP9P
FEMALE HOUSING
MALE PINS
TO MOTHERBOARD

CP9S
MALE HOUSING
FEMALE PINS
TO POWER SUPPLY

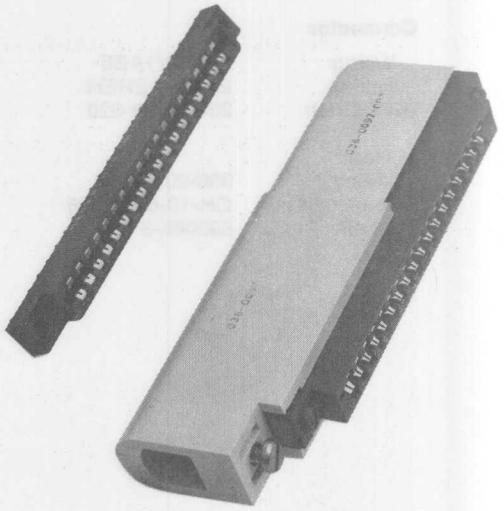
POWER CABLE COLOR CODE & PIN NUMBER		
FUNCTION	CABLE COLOR	PIN NO.
VCC	Red	1, 2
GND	Black	4, 5, 6
VBB	White	3
AUX +V	Orange	7
AUX GND	White/Black	8
AUX -V	Violet	9

	SOURCE FOR CONNECTOR AMP INC		
	DESCRIPTION	AMP PART NO.	NO. PER ASSY
CP9P	Connector-Cap 9 Position	Cap #350782-1	1
CP9P	Contact Pin	#350547-1	9
CP9S	Connector-Plug 9 Position	Plug #350720-1	1
CP9S	Contact Socket	#350550-1	9

CS18 I/O EDGE CONNECTOR

SOLDER TAIL CONNECTOR

The CS18 card edge connector is used on industrial interface cards requiring more than 50VDC and/or 0.5A per contact.

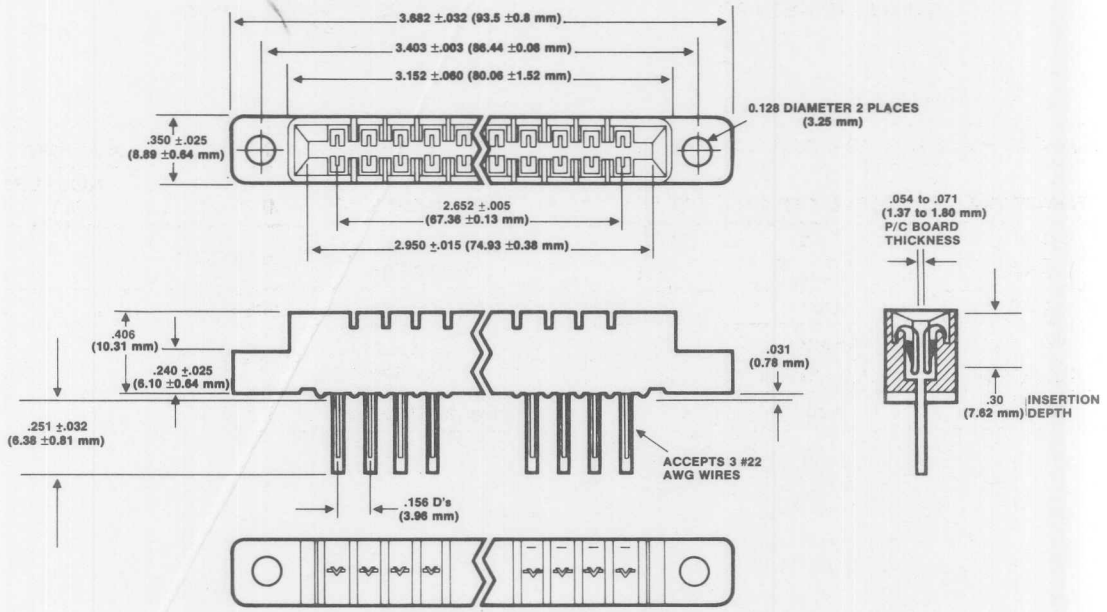


FEATURES

- **5A maximum per contact**
- **Multiple sourced**
- **Accepts PCBs of 0.062 in. (1.57 mm) thickness**
- **Pierced solder tails accept 3 #22 AWG wires**
- **Includes mating hood, hardware, and keys**
- **UL listed**

ELECTRICAL

- Material UL-rated 94V-0 or 94V-1 (flame rating)
- Contact spacing: 0.156 in (3.96 mm) centers
- Contact rating: 5A
- Maximum voltage drop: 30mV at 5A
- Operating voltage: 350V at sea level
- Operating temperature: -55°C to +105°C at sea level
- PCB thickness: 0.054 to 0.071 in. (1.37 to 1.80 mm)
- Insertion/withdrawal forces: 2 oz. to 8 oz. (0.56 to 2.24 N) per contact pair



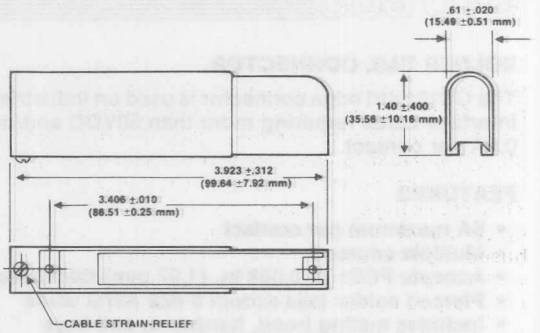
Solder Tail Connector

CS18 SOLDER TAIL CONNECTOR

ORDERING INFORMATION

Pro-Log CS18 includes connector, hood, hardware, and key. Part numbers given for other manufacturers are for connectors and hoods only.

Connector	
Viking	2VH18/1AB5
Sullins	EMM18 SREH
TRW Cinch	250-18-30-220
Hood	
Viking	036-0097-002
Kel-Am	CH-18-6H-3.406
AMP	530088-3



Typical Hood with Cable Clamp

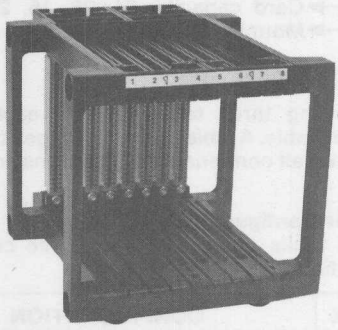
7000
STD BUS

BR-, ER-, & WR-SERIES CARD RACKS

The Pro-Log card racks are assembled from modular elements, allowing the designer a wide choice of rack designs. The four-slot card-rack modules are made from injection molded, glass filled, thermoplastic polycarbonate. They are assembled with mounting hardware in 36 different basic models. This allows the system designer an even wider range of card rack implementations, using a full-width bused motherboard, or one or more less-than-full-width bused motherboards in combination with unwired, wirewrap card-edge connectors.

These card racks accept all 4.5 by 6.5 in. (114.3 x 165.1 mm) STD BUS circuit cards and feature improved convection cooling.

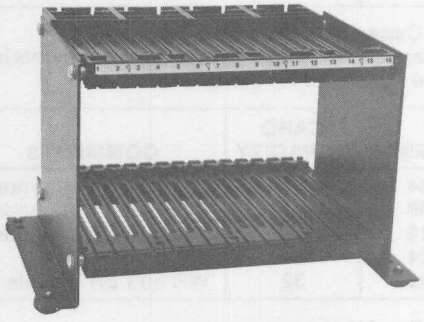
Card spacing is on 0.5 in. (12.7 mm) centers, except for the BR24 models, which have 16 card slots on 0.5 in. (12.7 mm) centers and 8 card slots on 1.0 in. (25.4 mm) centers.



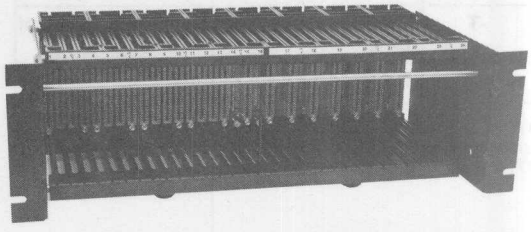
WR8-H

FEATURES

- **Accepts all STD BUS cards**
- **Available in 4, 8, 16, 24, and 32 card slot configurations**
- **Card spacing on 0.5 in (12.7 mm) centers (except BR24)**
- **Rugged, glass-filled thermoplastic construction**
- **Variety of mounting options: top, bottom, front, rear, and sides**
- **Variety of card-edge connector options: bused motherboards, wirewrap, or no connectors**
- **Wide temperature range: -15 to +85°C**



ER16-T

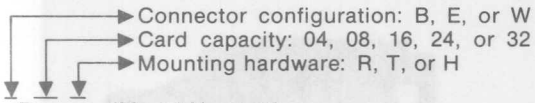


BR24-R

BR-, ER-, & WR- SERIES CARD RACKS

Model Number

The Pro-Log card racks are designated by a model number according to the following scheme:



The following three tables explain each of the options available. A table on the last page of this data sheet shows all combinations of options and model numbers.

Connector Configurations

The card racks are available in three connector configurations:

PREFIX	CONFIGURATION
BR	Edge connectors, bused motherboard, and power cable installed
WR	Unwired 56-pin wirewrap card-edge connectors installed
ER	No card-edge connectors installed

Card Capacity

The card capacity is indicated by the numerals in the middle of the model designation:

NUMBER	CARD CAPACITY	COMMENTS
04	4	Available in all models
08	8	Available in all models
16	16	Available in all models
24	24	BR models only
32	32	WR and ER models only

Mounting Hardware

Three mounting options are available, designated by the suffix:

SUFFIX	MOUNTING HARDWARE
-R	RETMA type, front rack mount [1]
-T	Table mount brackets at bottom of rack
-H	Pro-Log handle mounts

[1] These units have an overall height of 5.75 in. (146.1 mm) excluding feet, and are designed to fit in a RETMA standard 7 in. (177.8 mm) high panel space.

CARD RACK MOUNTING

The Pro-Log card racks can be used free-standing on their rubber feet, or they can be attached to a chassis or cabinet in a variety of ways, as described below.

Options for All Models

1. Use the racks free-standing on the factory-installed rubber feet.

or

2. Secure the racks through the holes provided on the top and bottom of the four-slot card rack modules. Four holes are provided on both the top and bottom of each module. Use #4-40 or similar self-tapping screws to secure the racks.

> CAUTION
>
> If the racks are mounted in this manner, provide for adequate airflow for convection cooling of the cards. Use spacers between the card racks and the panel to which they are secured, or provide openings in the panel if the racks are flush-mounted to it.

or

3. Attach the card racks through the slots on the rear faces of the four-slot card rack modules. Two slots are provided on both the top and bottom of each module.

Options for -R Models (RETMA type rack mount)

4. Mount the -R model card racks, using options 1 through 3, or mount the racks by the front mounting angle brackets. The brackets have mounting slots spaced on 4.0 in. (101.6 mm) centers on each side of the racks. These slots correspond to the standard RETMA dimensions for mounting 7 in. (177.8 mm) panels in 19 in. (482.6 mm) racks. The BR24-R, ER32-R, and WR32-R mount directly in a standard 19 in. (482.6 mm) RETMA rack.

Options for -T Models (tabletop type rack mount)

5. Mount the -T model card racks, using options 1 through 3, or mount by the bottom mounting angle brackets. Each bracket has four mounting holes, of which two are used to secure the rubber feet to the bracket.

Options for -H Models (Pro-Log handle type mount)

6. Mount the -H model card racks, using options 1 through 3, or mount them by either or both sides, using #10-32 screws to attach to the rack at the captive, threaded hexagonal inserts in the handles. The racks are shipped with all inserts on one side. But the user can reverse half of all the screws and inserts to provide two mounting points on each side, or four points on one side.

> NOTE
>
> The BR24, WR32, and ER32 cannot be mounted this way, since screws are used at both ends.

ENVIRONMENTAL SPECIFICATIONS

SYMBOL	PARAMETER	RECOMMENDED OPERATING LIMITS			ABSOLUTE NONOPERATING LIMITS		
		MIN	TYP	MAX	MIN	MAX	UNIT
T_A	Free air temp.	-15	+25	+85	-15	+85	°C
—	Humidity [1]	5	-	95	5	95	%RH

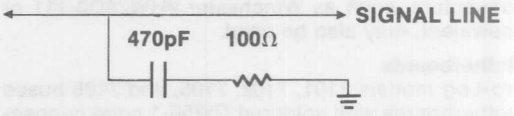
[1] Noncondensing

UL Rating: 94V-0

The recommended cleaning solvent is water or isopropyl alcohol.

LOGIC BUS TERMINATION (BR24 series with 7106 motherboard only)

The Pro-Log BR24 series card racks use passive AC termination on all signal lines (pins 7 through 50) to reduce electrical ringing. Undesired high frequency ringing is effectively terminated to the characteristic impedance of the motherboard. The steady-state DC drive of each output driver is not reduced by this circuit. The following circuit represents each of the bused signal terminations.



POWER CABLE SPECIFICATIONS

SYMBOL	BUS PINS	POWER CABLE		RECOMMENDED CURRENT (A)			
				BR04, BR08, BR16		BR24	
		PINS	COLOR	MAX	MIN	MAX	MIN
V_{cc}	1 & 2	1 & 2	Red	12.0	0.1	17.0	0.1
V_{bb}	5 [1]	3	White	1.0	0.1	1.0	0.1
V_{bb}	6 [1]	3	White	1.0	0.1	1.0	0.1
GND	3 & 4	4, 5, 6	Black	12.0	0.1	17.0	0.1
AUX +V	55	7	Orange	6.0	0.1	7.0	0.1
AUX -V	56	9	Violet	6.0	0.1	7.0	0.1
AUX GND	53 & 54	8	Wht/Blk	6.0	0.1	7.0	0.1

[1] V_{bb} (-5V) can be jumpered to pins 5 and/or 6 by user-installed jumpers on the motherboard. The BR24 comes with -5V already jumpered to pins 5 and 6.

Power Cable and BUS Specifications for BR Series Only.

DESCRIPTION	AMP PART NO.	NO. PER ASSY
Connector socket, 9-position	350782-1	1
Connector pin	350547-1	9
Connector plug, 9-position	350720-1	1
Contact socket	350550-1	9

Source for Connectors - AMP, INC.

ACCESSORIES

Edge Connector
Pro-Log model CW56 wirewrap edge connectors are available for use with the ER series card racks. For details, see the CW56 data sheet. User-supplied connectors, such as Winchester #HW28D0-111 or equivalent, may also be used.

Motherboards
Pro-Log models 7101, 7102, 7105, and 7106 bused motherboards with soldered CW56-1 edge connectors are available for use with the ER series card racks. For details, see the 7101, 7102, and 7105 data sheets, or the 7106 data sheets.

Wirewrap Kits
The Pro-Log model WK-1 wirewrap kit is available for making connections between the CW56 edge connectors used with the WR series card racks. For details, see the CW56 data sheet.

Power Supply Cables
The Pro-Log model CP9P nine-pin locking power connector with a 12 in. (304.8 mm) cable is available for connecting to the WR and ER series card racks. (The cable and connector are included with BR series card racks.) A mating CP9S connector and 12 in. (304.8 mm) cable are available for use with customer-provided power supplies. For details, see the CP9P/CP9S data sheet.

REFERENCES

Card Temperature Considerations
For information on card temperature considerations, request Pro-Log Application Note (PLAN) #133, Document #106257.

Power and Grounding Considerations
For information on system power and ground considerations, request Pro-Log Application Note (PLAN) #134, Document #106339.

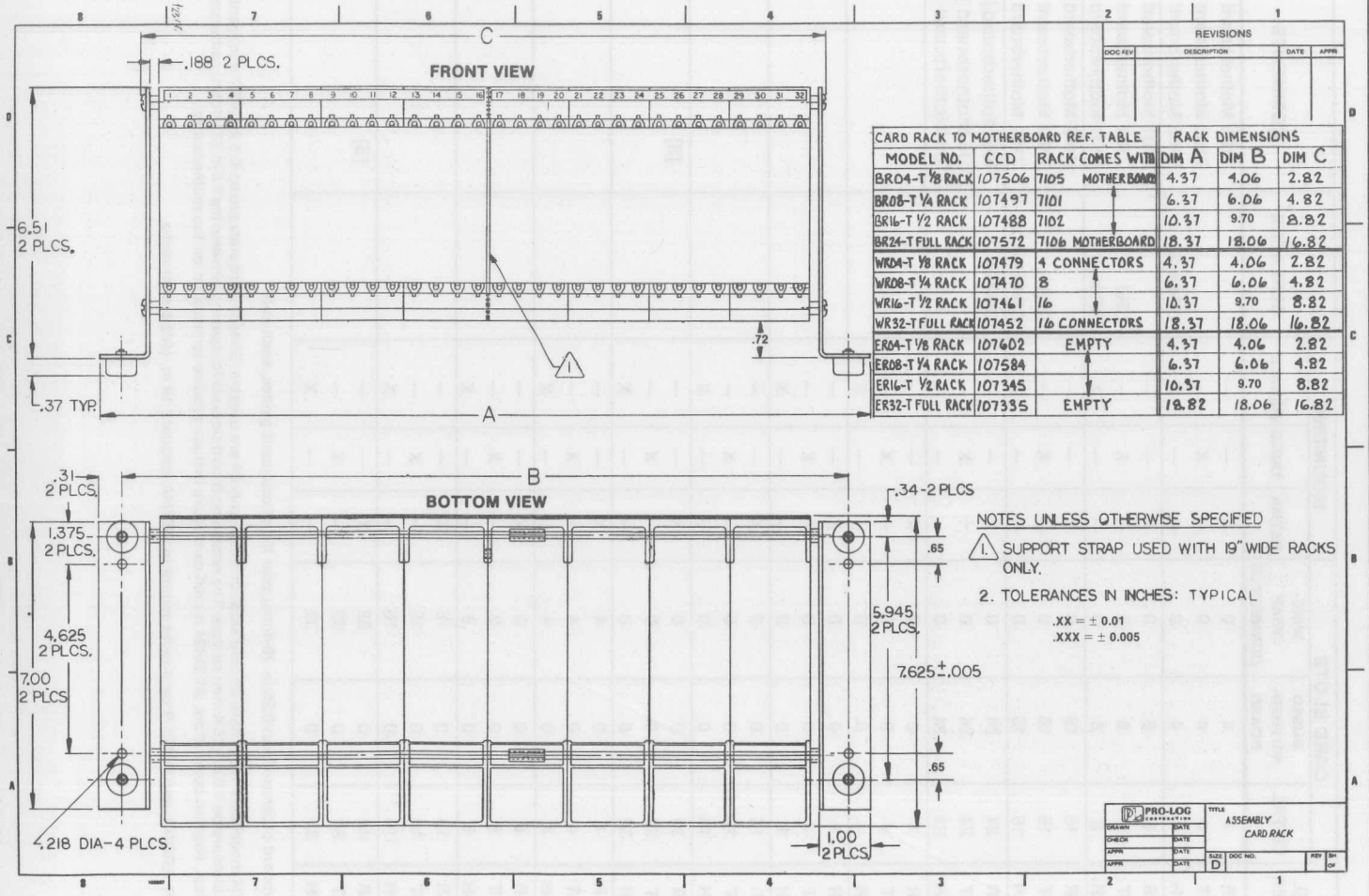
Card Rack User's Manual
To obtain the Pro-Log User's Manual for all Pro-Log series card racks, request Document #(pending).

MODEL NUMBER	CARD SLOTS			MOUNTING			REPLACES	COMMENTS
	TOTAL	BUSED MOTHER-BOARD	WIRE-WRAP CONNECTOR	RETMA	TABLE	HANDLE		
BR04-R	4	4	0	X	—	—		7105 Motherboard [1]
BR04-T	4	4	0	—	X	—		7105 Motherboard [1]
BR04-H	4	4	0	—	—	X	CR4A-2	7105 Motherboard [1]
BR08-R	8	8	0	X	—	—		7101 Motherboard [1]
BR08-T	8	8	0	—	X	—	CR8	7101 Motherboard [1]
BR08-H	8	8	0	—	—	X	CR8A-2	7101 Motherboard [1]
BR16-R	16	16	0	X	—	—		7102 Motherboard [1]
BR16-T	16	16	0	—	X	—	CR16	7102 Motherboard [1]
BR16-H	16	16	0	—	—	X	CR16A-2	7102 Motherboard [1]
BR24-R	24	24	0	X	—	—	CR24A	7106 Motherboard [2] [3]
BR24-T	24	24	0	—	X	—		7106 Motherboard [2]
BR24-H	24	24	0	—	—	X		7106 Motherboard [2]
ER04-R	4	0	0	X	—	—		
ER04-T	4	0	0	—	X	—		
ER04-H	4	0	0	—	—	X		
ER08-R	8	0	0	X	—	—		
ER08-T	8	0	0	—	X	—		
ER08-H	8	0	0	—	—	X		
ER16-R	16	0	0	X	—	—		
ER16-T	16	0	0	—	X	—		
ER16-H	16	0	0	—	—	X		
ER32-R	32	0	0	X	—	—		[3]
ER32-T	32	0	0	—	X	—		
ER32-H	32	0	0	—	—	X		
WR04-R	4	0	4	X	—	—		
WR04-T	4	0	4	—	X	—		
WR04-H	4	0	4	—	—	X		
WR08-R	8	0	8	X	—	—		
WR08-T	8	0	8	—	X	—		
WR08-H	8	0	8	—	—	X		
WR16-R	16	0	16	X	—	—		
WR16-T	16	0	16	—	X	—		
WR16-H	16	0	16	—	—	X		
WR32-R	32	0	32	X	—	—		[3]
WR32-T	32	0	32	—	X	—		
WR32-H	32	0	32	—	—	X		

[1] Motherboard projects about 0.25 in. (6.4mm) past the plastic card guides, each end.

[2] All BR24 model card racks have 32 card slots, of which only 24 are useable. Sixteen card slots are on 0.5 in. (12.7 mm) centers and 8 card slots are on 1.0 in. (25.4 mm) centers. The remaining 8 card slots are for spacing between the 1.0 in. (25.4 mm) center card slots and, thus, have no connectors. All BR24 model card racks include passive termination on the motherboard.

[3] BR24-R, ER32-R, and WR32-R card racks mount in RETMA standard 19 in. (482.6 mm) racks.



REVISIONS			
DOC REV	DESCRIPTION	DATE	APPR

CARD RACK TO MOTHERBOARD REF. TABLE			RACK DIMENSIONS		
MODEL NO.	CCD	RACK COMES WITH	DIM A	DIM B	DIM C
BR04-T 1/8 RACK	107506	7105 MOTHERBOARD	4.37	4.06	2.82
BR08-T 1/4 RACK	107497	7101	6.37	6.06	4.82
BR16-T 1/2 RACK	107488	7102	10.37	9.70	8.82
BR24-T FULL RACK	107572	7106 MOTHERBOARD	18.37	18.06	16.82
WR04-T 1/8 RACK	107479	4 CONNECTORS	4.37	4.06	2.82
WR08-T 1/4 RACK	107470	8	6.37	6.06	4.82
WR16-T 1/2 RACK	107461	16	10.37	9.70	8.82
WR32-T FULL RACK	107452	16 CONNECTORS	18.37	18.06	16.82
ER04-T 1/8 RACK	107602	EMPTY	4.37	4.06	2.82
ER08-T 1/4 RACK	107584		6.37	6.06	4.82
ER16-T 1/2 RACK	107345		10.37	9.70	8.82
ER32-T FULL RACK	107335	EMPTY	18.82	18.06	16.82

NOTES UNLESS OTHERWISE SPECIFIED

1. SUPPORT STRAP USED WITH 19" WIDE RACKS ONLY.
2. TOLERANCES IN INCHES: TYPICAL
   .XX = ± 0.01
   .XXX = ± 0.005

PRO-LOG CORPORATION		TITLE: ASSEMBLY CARD RACK	
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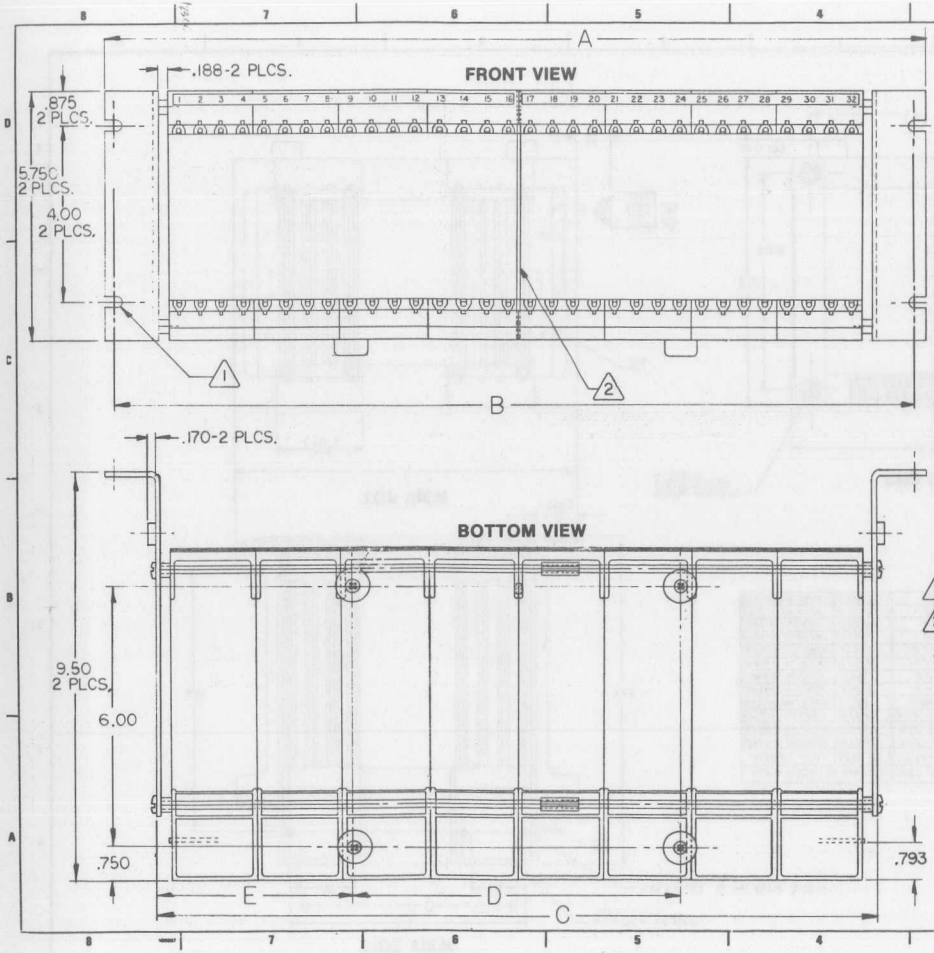
Envelope and Mounting Dimensions for -T Models



REVISIONS

DOC REV	DESCRIPTION	DATE	APPR

CARD RACK TO MOTHER'BD. REF. TABLE			RACK DIMENSIONS				
MODEL NO.	CCD	RACK COMES WITH	DIM A	DIM B	DIM C	DIM D	DIM E
BR04-R 1/8 RACK	107500	7105 MOTHER'BD	4.87	4.31	2.56	1.50	.25
BR08-R 1/4 RACK	107491	7101	6.87	6.31	4.56	3.50	.25
BR16-R 1/2 RACK	107482	7102	10.87	10.31	8.56	7.50	.25
BR24-R FULL RACK	106907	7106 MOTHER'BD.	18.87	18.31	16.56	7.50	4.25
WR04-R 1/8 RACK	107473	4 CONNECTORS	4.87	4.31	2.56	1.50	.25
WR08-R 1/4 RACK	107464	8	6.87	6.31	4.56	3.50	.25
WR16-R 1/2 RACK	107455	16	10.87	10.31	8.56	7.50	.25
WR32-R FULL RACK	107446	16 CONNECTORS	18.87	18.31	16.56	7.50	4.25
ER04-R 1/8 RACK	107608	EMPTY	4.87	4.31	2.56	1.50	.25
ER08-R 1/4 RACK	107590		6.87	6.31	4.56	3.50	.25
ER16-R 1/2 RACK	107434		10.87	10.31	8.56	7.50	.25
ER32-R FULL RACK	107436	EMPTY	18.87	18.31	16.56	7.50	4.25

NOTES: UNLESS OTHERWISE SPECIFIED

1. MOUNTING SLOTS ARE .250 DIA.-4 PLCS.
2. SUPPORT STRAP USED WITH 19" WIDE RACKS ONLY.
3. TOLERANCES IN INCHES: TYPICAL

.XX = ± 0.01

.XXX = ± 0.005

PRO-LOG	TITLE: ASSEMBLY CARD RACK
DRAWN / DATE	
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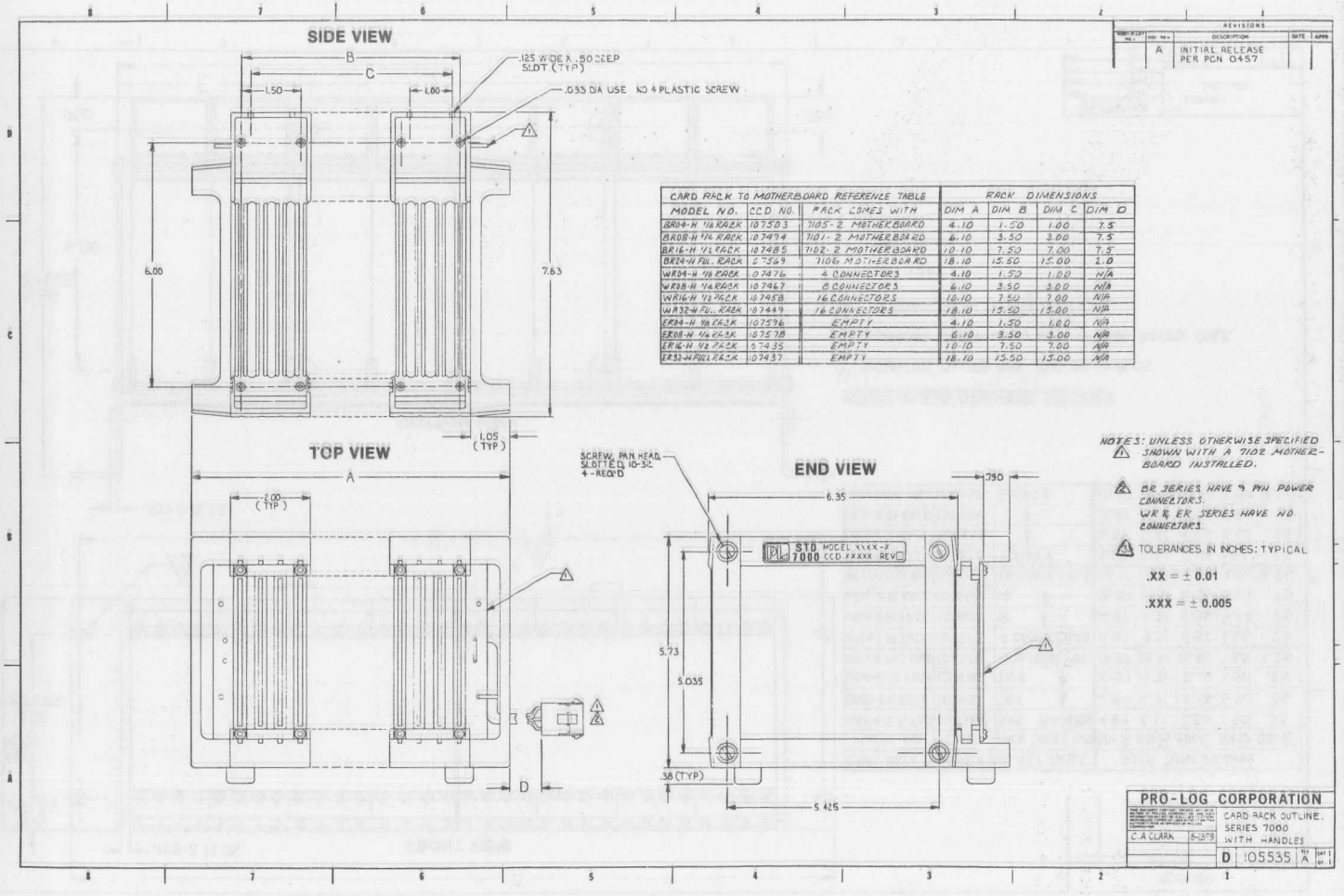
APPR / DATE	
APPR / DATE	SIZE D · DOC NO. · REV · SH OF

Envelope and Mounting Dimensions for -R Models



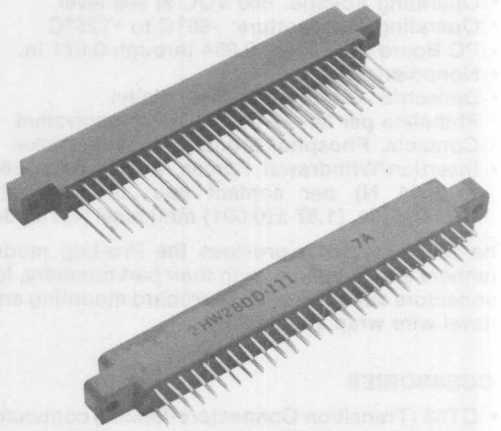
CARD RACK TO MOTHERBOARD REFERENCE TABLE			RACK DIMENSIONS			
MODEL NO.	CCD NO.	RACK COMES WITH	DIM A	DIM B	DIM C	DIM D
BR04-H 1/8 RACK	107503	7105-2 MOTHERBOARD	4.10	1.50	1.00	7.5
BR08-H 1/4 RACK	107494	7101-2 MOTHERBOARD	6.10	3.50	3.00	7.5
BR16-H 1/2 RACK	107485	7102-2 MOTHERBOARD	10.10	7.50	7.00	7.5
BR24-H FUL. RACK	107569	7106 MOTHERBOARD	18.10	15.50	15.00	2.0
WR04-H 1/8 RACK	107476	4 CONNECTORS	4.10	1.50	1.00	N/A
WR08-H 1/4 RACK	107467	8 CONNECTORS	6.10	3.50	3.00	N/A
WR16-H 1/2 RACK	107458	16 CONNECTORS	10.10	7.50	7.00	N/A
WR32-H FUL. RACK	107449	16 CONNECTORS	18.10	15.50	15.00	N/A
ER04-H 1/8 RACK	107536	EMPTY	4.10	1.50	1.00	N/A
ER08-H 1/4 RACK	107578	EMPTY	6.10	3.50	3.00	N/A
ER16-H 1/2 RACK	107435	EMPTY	10.10	7.50	7.00	N/A
ER32-H FULL RACK	107437	EMPTY	18.10	15.50	15.00	N/A

Envelope and Mounting Dimensions for -H Models

7000
STD BUS

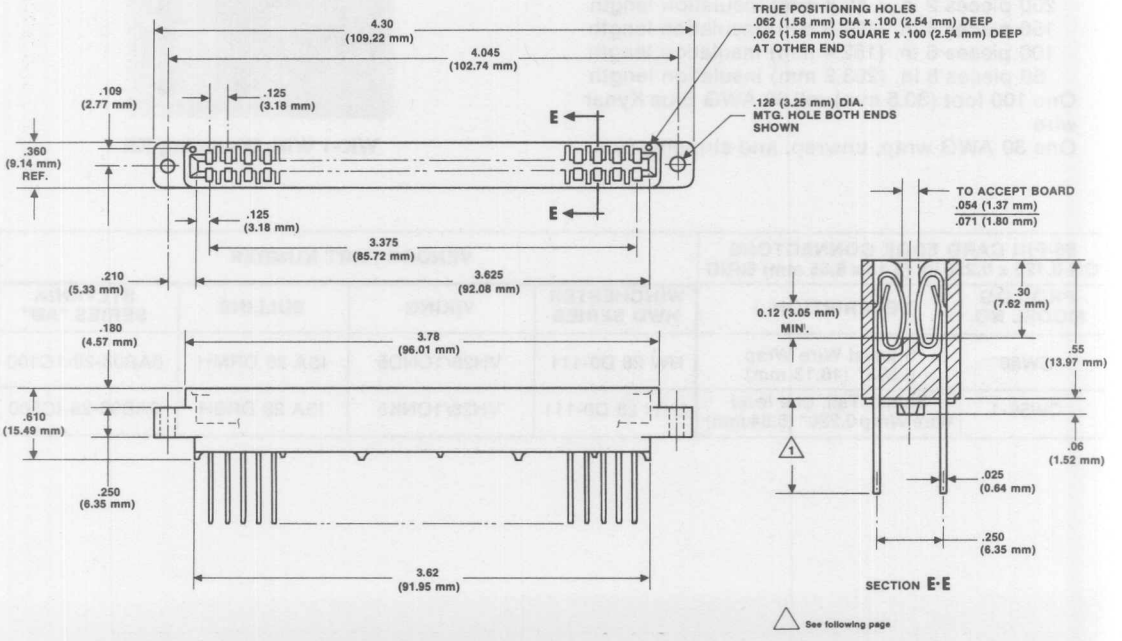
CW56-0, CW56-1
EDGE CARD CONNECTORS

The CW56 and CW56-1 are card edge, 56-pin connectors. The CW56 is a 3-level wire wrap connector with 0.025 in. (0.64 mm) square wire wrap post on 0.125 in. (3.18 mm) centers. The CW56-1 is a solder tail version of the same connector.



FEATURES

- **3A per contact**
- **Accepts 0.062 in. (1.58 mm) thick PCBs**
- **Multiple sourced**

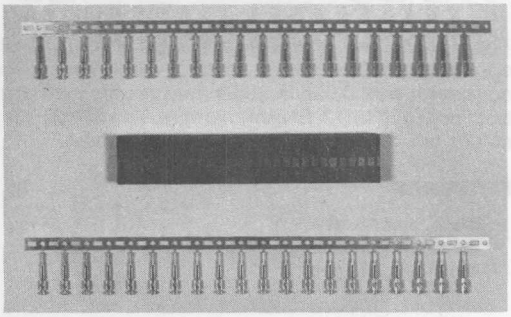


CW56, CW56-1 EDGE CARD CONNECTORS

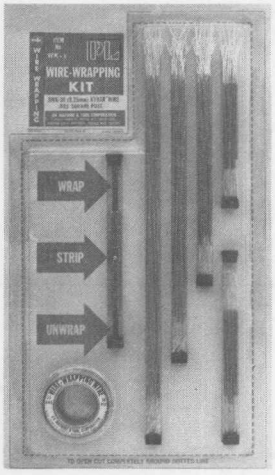
Requirements for 56-pin Edge Card Connector 0.125 x 0.250 in. (3.18 x 6.35 mm) grid spacing:

- Current Rating: 3A per contact
- Max Voltage Drop: 30mV at 3 A per contact
- Operating Voltage: 600 VDC at sea level
- Operating Temperature: -65°C to +125°C
- PC Board thickness: 0.054 through 0.071 in.
- Nonpolarized
- Dielectric: Green glass-filled diallyl
- Phthalate per Mil-M-14, SDG-F or equivalent
- Contacts: Phosphor bronze, gold over nickel
- Insertion/Withdrawal Forces: 2 to 8 oz (0.56± to 2.24 N) per contact pair, using 0.062± (0.00005) in. [1.57 ±(0.001) mm] steel test blade.

The following table provides the Pro-Log model numbers and suppliers, with their part numbers, for connectors suitable for motherboard mounting and 3-level wire wrap applications.



CT56 Transition Connector



WK-1 Wire Wrapping Kit

ACCESSORIES

- CT56 (Transition Connectors-female) connector that slides on CW56 wire wrap post and connects to discrete wires via selfcrimp connections.
- The WK 1 wire wrapping kit provides wire and a tool for wire wrapping, unwrapping, and stripping.

The Kit includes:

Precut and stripped 30 AWG Blue Kynar wire.
200 pieces 2 in. (50.8 mm) insulation length
150 pieces 4 in. (101.6 mm) insulation length
100 pieces 6 in. (152.4 mm) insulation length
50 pieces 8 in. (203.2 mm) insulation length
One 100 foot (30.5 mm) roll 30 AWG Blue Kynar wire
One 30 AWG wrap, unwrap, and stripping tool

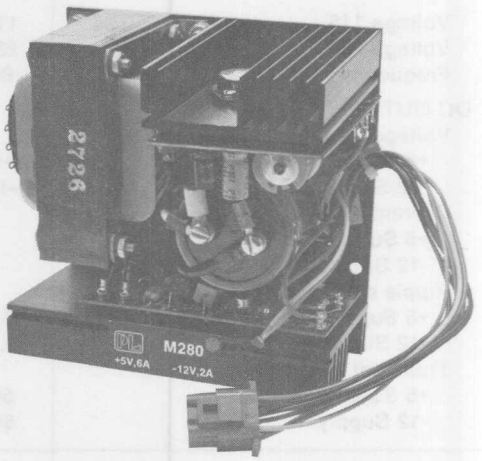
56-PIN CARD EDGE CONNECTORS ON 0.125 x 0.250 in. (3.18 x 6.35 mm) GRID		VENDOR PART NUMBER			
PRO-LOG MODEL NO.	DESCRIPTION 1	WINCHESTER HWD SERIES	VIKING	SULLINS	SYLVANIA SERIES "AB"
CW56	3-Level Wire Wrap 0.635" (16.13 mm)	HW 28 D0-111	VH28/1CND5	ISA 28 DRMH	6AB03-28-1C100
CW56-1	Solder Tail, one level Wire Wrap 0.230" (5.84 mm)	2HW 28 D0-111	VH28/1CNK5	ISA 28 DRSH	6AB03-28-IC500

7000
STD BUS

M280
DUAL OPEN FRAME POWER SUPPLY

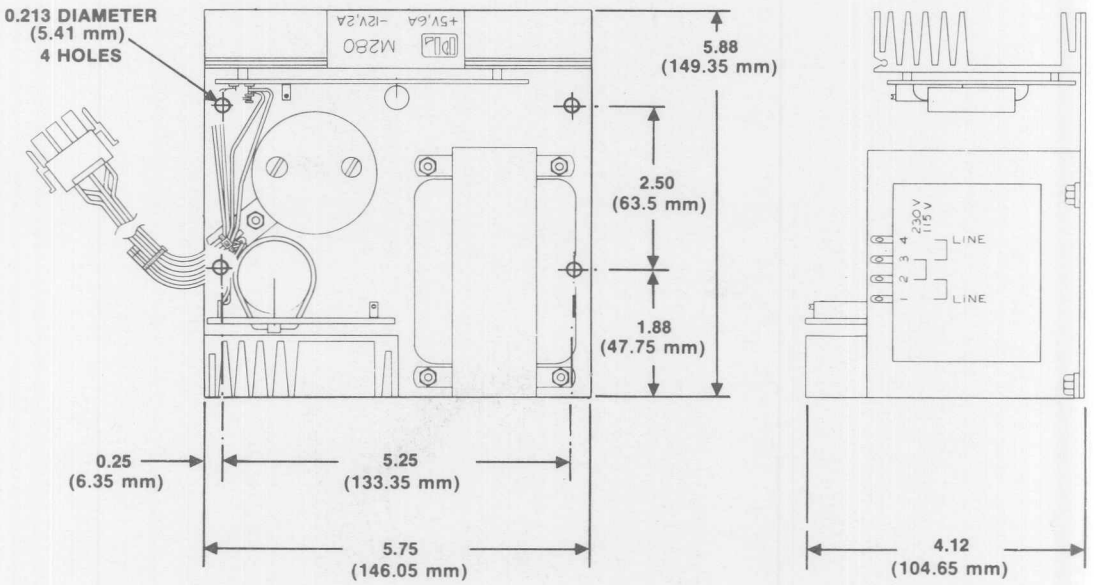
The M280 is a dual open-frame power supply assembly providing +5V/6A and -12V/2A. The assembly is shipped with a 12 in. (304.8 mm) DC output cable and 9-pin keyed and locking power connector (CP9P) and mates with the 7100 Series Motherboards and CR Series Card Racks. Both supplies are current-limited for short-circuit protection.

The M280 is shipped without AC line cord, switch, or fusing. These items are supplied by the user.



FEATURES

- **+5V/6A with current-limiting**
- **-12/2A with current-limiting**
- **Open-frame power supply**
- **User-added AC power wiring**



M280 Power Supply Assembly

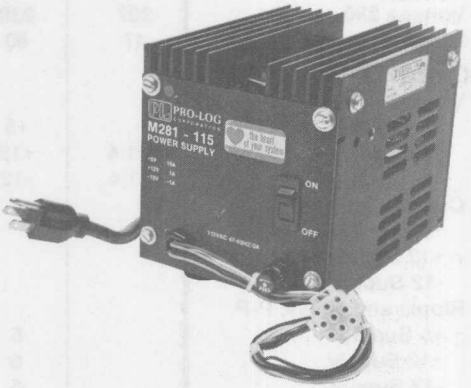
M280 DUAL OPEN FRAME POWER SUPPLY

ELECTRICAL

PARAMETER 0°C to 55°C	MIN	TYP	MAX	UNIT	COMMENT
AC INPUT					
Voltage 115	103.5	115	126.5	V	Voltage strapping option
Voltage 230	207	230	253	V	
Frequency	47	60	63	Hz	
DC OUTPUT					
Voltage					
+5 Supply		+5		V	Adjustable
-12 Supply		-12		V	
Current, Max					
+5 Supply			6	A	
-12 Supply			2	A	
Ripple and Noise, P-P					
+5 Supply		0.1		%	
-12 Supply		0.1		%	
Transient Response					
+5 Supply		50		μs	For 50% load change
-12 Supply		50		μs	For 50% load change
ENVIRONMENTAL					
Operating temp. range	0		+55	°C	Derated from +55°C
Storage temp.	-25		+85	°C	2%/°C to +70°C
Humidity	5		90	%	Noncondensing

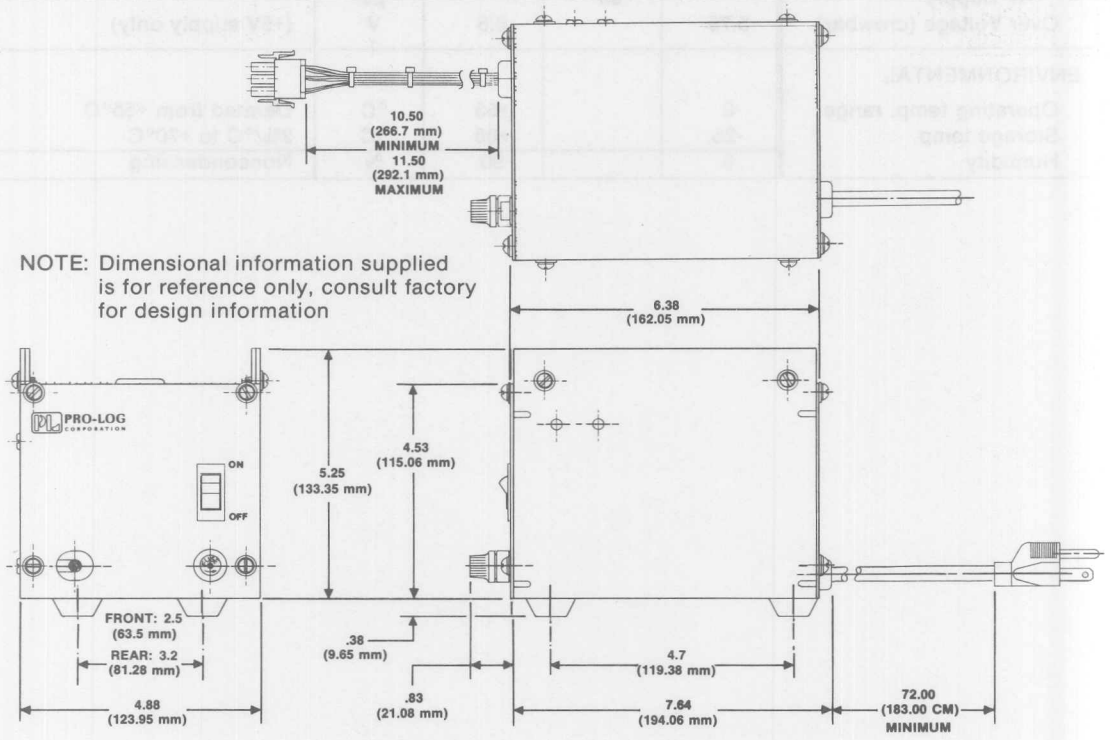
7000 STD BUS M281 TRIPLE POWER SUPPLY ASSEMBLY

The M281 is an enclosed, triple power supply assembly providing +5V/10A and **±12V/1A each. The assembly is complete with a 6-foot AC line cord, power switch, and fuse. A one-foot DC output cable and 9-pin keyed and locking power connector (CP9P) mates with the 7100 Series Motherboards and CR Series Card Racks. All three supplies are current-limited for short circuit protection, and the +5V supply features output voltage adjustment and over-voltage protection.**



FEATURES

- **+5V/10A with over-voltage protection**
- **±12V/1A each**
- **Completely assembled and ready to operate**
- **Order M281-115 for 115 VAC version, or M281-230 for 230 VAC version with tandem blade AC plug**



Typical M281 Power Supply Assembly

M281 TRIPLE POWER SUPPLY ASSEMBLY

ELECTRICAL

PARAMETER 0°C to 55°C	MIN	TYP	MAX	UNIT	COMMENT
AC INPUT					
Voltage 115	103.5	115	126.5	V	
Voltage 230	207	230	253	V	Optional
Frequency	47	60	63	Hz	
DC OUTPUT					
Voltage					
+5 Supply		+5		V	Adjustable -5% to +15%
+12 Supply	+11.4	+12	+12.6	V	Fixed (no load)
-12 Supply	-11.4	-12	-12.6	V	Fixed (no load)
Current, Max					
+5 Supply			10	A	
+12 Supply			1	A	
-12 Supply			1	A	
Ripple and Noise, P-P					
+5 Supply		5		mV	
+12 Supply		5		mV	
-12 Supply		5		mV	
Transient Response					
+5 Supply		50		μs	
+12 Supply		50		μs	
-12 Supply		50		μs	
Over Voltage (crowbar)	5.75		6.5	V	(+5V supply only)
ENVIRONMENTAL					
Operating temp. range	0		+55	°C	Derated from +55°C
Storage temp.	-25		+85	°C	2%/°C to +70°C
Humidity	5		90	%	Noncondensing

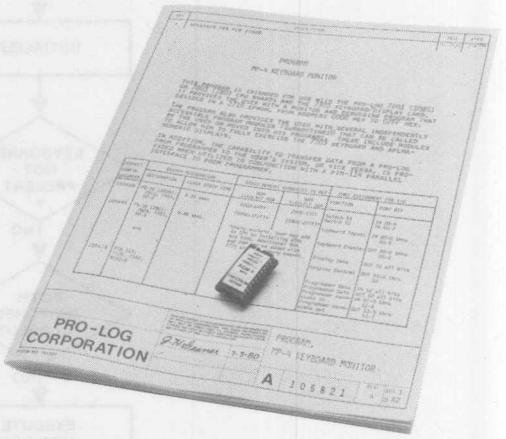
7000 STD BUS

MP4 MONITOR PROGRAM

The MP4 monitor program is an STD BUS program development and debugging tool designed for use with the 7303 keyboard/display card. It is programmed in a 2716 EPROM and includes: program listings, flow diagrams, memory maps, and operating instructions. The program is for use with the 8085 and Z80.

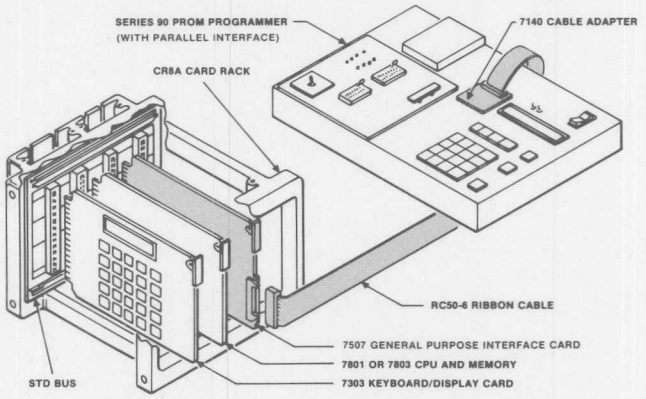
The MP4 allows the designer/engineer to develop, execute, debug, and modify a program in RAM memory. Also included is software that allows data transfer between system memory and any Pro-Log PROM programmer equipped with a parallel interface 9104, 9114, or 9814. The interface can be implemented by the addition of the PIN114 parallel interface for STD BUS prototyping systems.

The MP4 can also double as a diagnostic tool, resident in the user's system. If both toggle switches on the 7303 keyboard/display card are closed or if the 7303 is not present, program control is transferred directly to address 0800 hexadecimal and the monitor is bypassed. In addition, several routines are incorporated to complement hardware/software debugging with the Pro-Log M824 (Z80) and M825 (8085A) system analyzers.



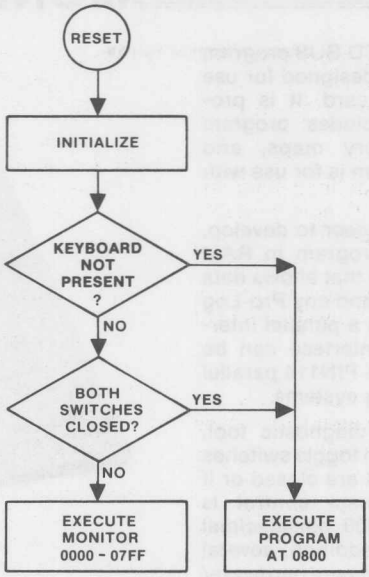
FEATURES

- **Available for use with Z80 and 8085A CPUs**
- **Resident in one 2716 EPROM**
- **Program list and execute programs in RAMs**
- **Preset registers and set breakpoints**
- **Displays register contents at breakpoint or by analyzer-generated nonmaskable interrupt**
- **I/O driver for series 90 PROM programmers**
- **Moves data with address translation**
- **Most restart locations are unprogrammed and available to user**
- **Restart 7 (FF): jump to RAM-based, user-defined interrupt vector**
- **Contains RAM test with bad address identification**
- **Full user prompting with alphanumeric displays**



Suggested Hardware for MP4 Monitor Program

(The shaded assemblies depict the Parallel Interface PIN114.)



Monitor Operating System

MONITOR PROGRAM COMMAND SET

Edit
EDT—Display address and data from memory, beginning at user-defined address and listing forward or backward through memory. Modify RAM contents while listing, if desired.

Breakpoint Set
BPT—Set a breakpoint at user-defined address. Register contents displayed in 7303 alphanumeric displays upon execution of breakpoint.

Execution Address
XAD—Enter address at which execution is to begin upon selecting RUN. Execution will always begin at the entered address until changed.

Run
RUN—Begin execution, starting at previously entered address with registers preloaded with values entered into RAM by the STR command.

Set Registers
STR—Preset values in RAM from keyboard for subsequent loading into registers each time RUN is selected.

Send
SND—Transfer data from the user's system to the PROM programmer. The user defines the PROM beginning and ending addresses, and beginning system address.

Receive
RCV—Transfer data from the PROM programmer to the user's system. The user defines the PROM beginning and ending addresses, and beginning system address.

Move
MOV—Move data that resides between and includes the user-defined limits to the user-defined destination. Forward and backward moves are permitted. At completion of move, source memory locations are set to 00 hexadecimal.

Fill Memory
FLM—Fill all memory locations between the user-defined limits, inclusively, with the data byte entered from the keyboard. Stop and display the address and resident data of any location that does not successfully accept the user-entered data.

Adjust Addresses
AJA—Adjust all 3-byte jump and load instruction addresses affected by the last MOV operation by adding or subtracting the move offset. User defines the address limits over which adjustment is to be made.

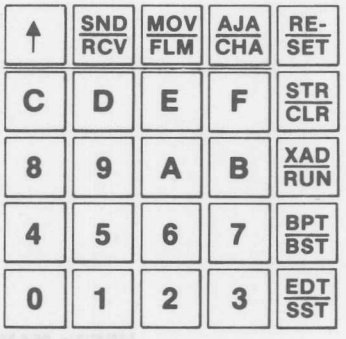
Change Addresses
CHA—Change all 3-byte jump and load instruction addresses within the user-defined limits by adding an offset. The user defines the address limits in which the program is intended to operate, and the beginning address of the area of memory in which the user would like it to operate.

Clear Entry
CLR—Clear the last digit of entered data or address from the display and permit a corrected entry.

Back Step
BST—Backstep through while listing from memory.

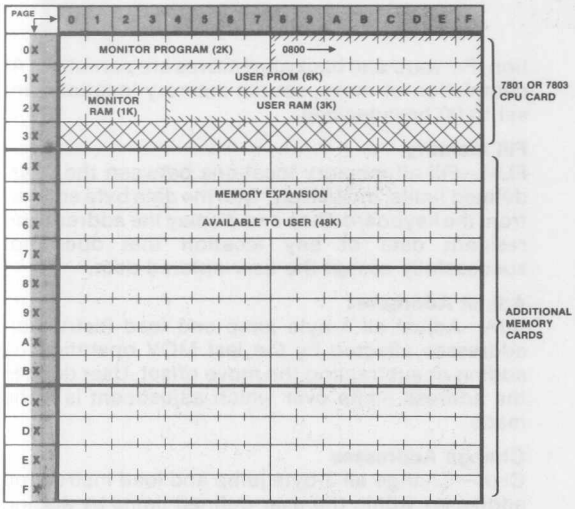
Single Step
SST—Used to enter address information and program data. Also used to single-step through memory while listing from memory.

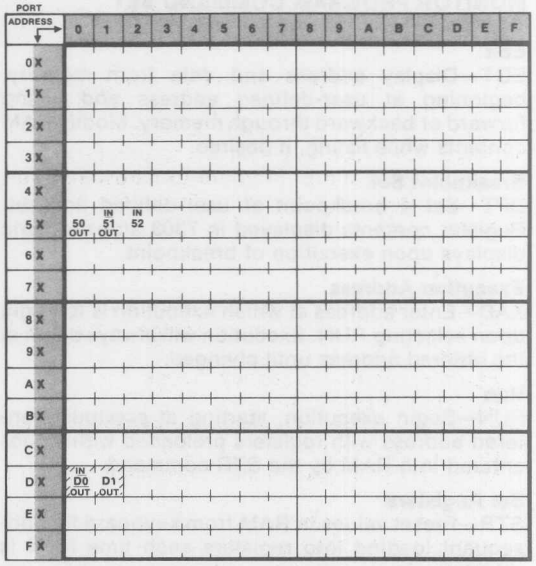
Upper Case
↑—Used to select upper case commands.



Monitor Program Keyboard

MP4 MONITOR PROGRAM





ORDERING INFORMATION

The monitor program and recommended hardware are available as prototyping systems. For additional information, refer to the PS1B and PS3B data sheets.

For further information on the PIN114, refer to the PIN114 data sheet.

The monitor program listing and the 7303 user's manual contain labeling instructions for monitor function keys.

USER's MANUAL

To obtain the user's manual for the MP4, ask for Pro-Log document #106821.

7000
STD BUS

TEST EQUIPMENT
M824, Z80 SYSTEM ANALYZER

The M824 system analyzer is a portable, cost-effective instrument that supports the design, development, production, and field service of Z80 microprocessor-based systems. The unit functions as a program monitor, program-to-hardware integrator and provides many of the display functions of a computer control panel.

FEATURES:

- **Tests systems using the Z80 microprocessor**
- **Displays address, data, machine cycle, and status**
- **Static and dynamic display modes**
- **System run/step control**
- **Connects to processor chip via clip-on or low-profile connector**
- **Oscilloscope trigger at address compare or data display time**
- **Delayed data capture**
- **Memory or I/O address select**
- **Nonmaskable interrupt capability at address compare**
- **External control of data display**
- **Address stop**
- **Interrupt trap and display**
- **Interface buffer to minimize microprocessor loading**

M824, System Analyzer in Case

- **High-impact attache case**
- **UL listed**

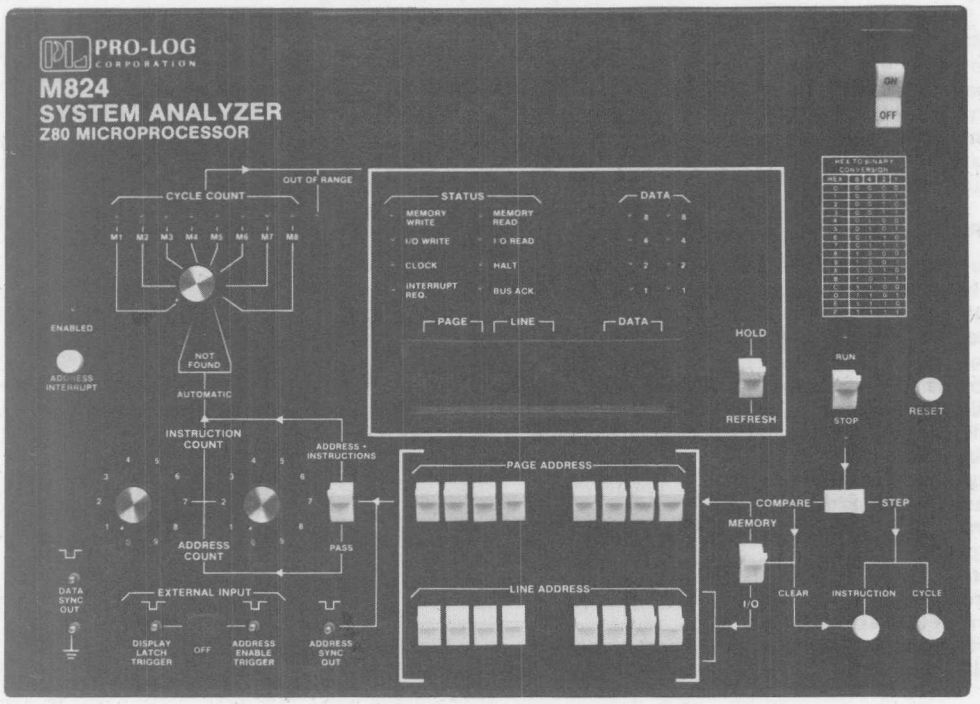
The M824 is self-contained and easily connected to your system microprocessor by means of a single DIP clip or low profile connector. It is useful as an alternative or complement to software techniques for program development or debugging of Z80-based microprocessor systems. Since it is easily connected, the M824 system analyzer, together with adequate program documentation, is an ideal tool for field service or production.

The analyzer allows examination of the system (address, data, and status) during a user-specified machine cycle at the desired compare address. Observation of the system is possible at full system speed or by single step-by-step instruction or machine cycle. The possible display modes are dynamic mode, in which the processor continues to run without analyzer interference, and static mode, in which the analyzer controls the processor WAIT line.

Delayed data capture affords the capability of observing a particular machine cycle up to 99 instructions past a chosen reference address. The feature also allows observing the reference address after a user-defined number of passes over that address. A two-decade address counter, coupled with a single machine cycle counter, provides the operator with the capability of simply "dialing" his way through the program under investigation. This delay capability may be extended to any number by utilizing stop/compare mode.

The M824 provides memory or I/O address selection and interrupt trap and/or stop on interrupt, along with hexadecimal address, hexadecimal and binary data, and status displays. The analyzer also features an oscilloscope synchronization output pulse during address compare and data display latch time. DATA SYNC OUT can be utilized to trigger an oscilloscope at any selectable instruction cycle.

Operator-initiated functions include microprocessor push-button reset, latch display or latch display and stop at the next T2 state after trigger, stop on next address compare after trigger, and generation of nonmaskable interrupt at address compare time.



M824, Front Panel

ADDRESS CONTROLS

ADDRESS switches: Sixteen address (bit) select toggle switches, broken into two groups: page address (high order address—A8 through A15) and line address (low order address or I/O—A0 through A7); used to establish the trigger reference address.

RUN/STOP switch: Selects dynamic mode (microprocessor continues to run) or static mode (microprocessor is stopped at data latch time and may be stepped through the program).

COMPARE/STEP switch: Is only functional in stop mode and selects stop on address compare and single step on cycle or instruction.

MEMORY I/O switch: Selects examination of data flow to/from memory location defined by page and line address switches, or I/O device defined by the low-order (line) address switches.

HOLD/REFRESH switch: Controls latching of the data display. In HOLD, the display is frozen the first time the selected compare condition is met. In REFRESH, the display is refreshed each time the selected compare condition is met.

DELAYED DATA CAPTURE CONTROLS

ADDRESS+INSTRUCTION/PASS Toggle switch: Address + instruction model allows data selection and display at an address up to 99 instructions beyond compare address. Pass mode allows up to 99 passes through a selected address before data is displayed.

ADDRESS COUNT/INSTRUCTION COUNT Rotary switch: Controls the number of address passes in pass mode, the number of additional instructions in address+instruction mode.

CYCLE COUNT Rotary switch: Selects machine cycle of interest.

ADDRESS INTERRUPT PUSH-BUTTON

ADDRESS INTERRUPT: Activation of this push-button will set an address compare latch and the next occurrence of address compare will generate a nonmaskagle interrupt. Appropriate interrupt service routines must be supplied by the user and located at the required memory location. If the analyzer is stopped by address compare, the interrupt will be generated immediately.

DISPLAYS:

ADDRESS: Displays 16-bit address as 4 hexadecimal digits within a range of 0000-FFFF.

DATA: A 2-digit hexadecimal display and two groups of 8 (bit) indicators, providing binary and hexadecimal data representation.

STATUS: Eight individual indicators showing data and machine status.

MEMORY READ/WRITE and I/O READ/WRITE: Indicate the function associated with the data being displayed.

CLOCK: Indicates the processor clock is operational.

INTERRUPT REQ: Indicates a system interrupt has occurred.

HALT: Indicates the processor is in the halt state.

BUS ACK: Indicates the processor has acknowledged and responded to a bus request.

RUN/STOP: Indicates status of the machine WAIT line; RUN for program execution, STOP for processor idle (WAIT state).

CYCLE COUNT: Machine cycle indicator showing the cycle of the instruction with which the displayed data is associated.

NOT FOUND: Indicates that the selected machine cycle was not found.

ENABLED: Indicates the address interrupt feature is enabled.

OUT-OF-RANGE: Indicates a machine cycle greater than eight is being displayed.

SYNC POINTS

ADDRESS SYNC OUT: Provides a negative pulse out for oscilloscope triggering each time the selected address compares with the system address lines.

DATA SYNC OUT: Provides a delayed negative pulse out for oscilloscope triggering each time the analyzer data display is latched. The delay is a function of the setting of address/ instruction + machine cycle count selectors.

DISPLAY LATCH TRIGGER IN: Each negative input edge causes the analyzer to latch data at the next T2 time. If the display selector is in the hold mode, address and data are latched for each negative edge and all address compare data is locked out. If the analyzer is in the stop mode, the system can thus be halted by the external event.

ADDRESS ENABLE TRIGGER IN: For each negative input edge, an address compare latch will be set and the next address compare occurring will stop the system via the WAIT line, whether or not the analyzer is in the run mode. Depressing CLEAR will release the system and reset the latch.

GROUND pin: Ground provided for all outputs and triggers.

USER SYSTEM REQUIREMENTS

The WAIT, RESET, and NMI lines must be capable of being wire-ORed. All interrupt lines must be strapped inactive if not used. A gate isolation resistance of 100Ω to 200Ω is recommended.

MAXIMUM μP CLOCK FREQUENCY: 4.0 MHz

LOADING SPECIFICATIONS

Inputs:

Address, data INT, clock, and system control lines	0.125 TTL loads @ 50 pF
WAIT, RESET	1.6 TTL loads @ 100 pF
NMI	0.125 TTL loads @ 100 pF
Display latch and address enable trigger	1.6 TTL loads @ 50 pF

Outputs:

WAIT, RESET	8 TTL loads
NMI	ON: Source 40 mA (min) to +5V OFF: Open circuit
Address and data sync out	1 TTL load

POWER REQUIREMENTS

50/60 Hz 115 VAC @ 0.75 A, or
50/60 Hz 230 VAC @ 0.300 A

PHYSICAL CHARACTERISTICS

Analyzer Control Unit
Height - 4.5 in. (114.3 mm)
Width - 21 in. (533.4 mm)
Length - 12 in. (304.8 mm)

Buffer Module and Cables
Height - 1.125 in. (28.58 mm)
Width - 2.5 in. (63.5 mm)
Length - 4.5 in. (114.3 mm)

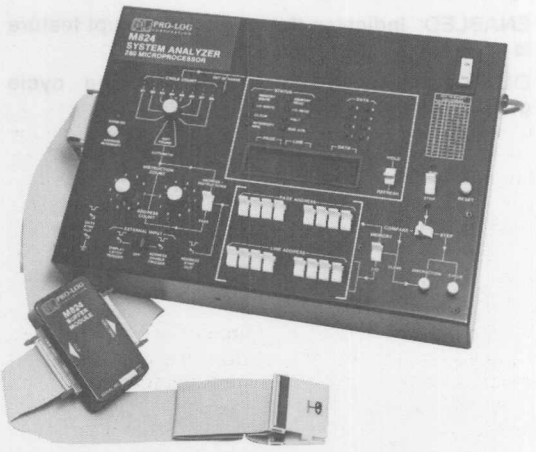
Attaché Case
Height - 6.5 in. (165.1 mm)
Width - 12.5 in. (317.5 mm)
Length - 23 in. (584.2 mm)

Total product weight is less than 15 pounds (6.80 kg).

OPERATING TEMPERATURE: 0°C to +45°C

M824 INCLUDES:

- Analyzer control unit
- Plug-in buffer module and cable
- 40-pin DIP clip connector assembly
- 40-pin low-profile connector assembly
- Attaché case
- Two copies of operating manual



USER's MANUAL

To obtain the user's manual for the M824, ask for Pro-Log document #105331.

7000
STD BUS

TEST EQUIPMENT
M825, 8085(A) SYSTEM ANALYZER

The M825 system analyzer is a portable, cost-effective instrument that supports the design, development, production, and field service of 8085 and 8085A microprocessor-based systems. The unit functions as a program monitor, program-to-hardware integrator and provides many of the display functions of a computer control panel.

FEATURES:

- **Tests systems using the 8085 or 8085A microprocessor**
- **Displays address, data, machine cycle, and status**
- **Static and dynamic display modes**
- **System run/step control**
- **System reset push-button**
- **Connects to processor chip via clip-on or low-profile connector**
- **Oscilloscope trigger at address compare or data display time**
- **Delayed data capture**
- **Memory or I/O address select**
- **Nonmaskable interrupt capability at address compare**
- **External control of data display**
- **Address stop**
- **Interrupt trap and display**

M825, System Analyzer in Case

- **Interface buffer to minimize microprocessor loading**
- **High-impact attaché case**
- **UL listed**

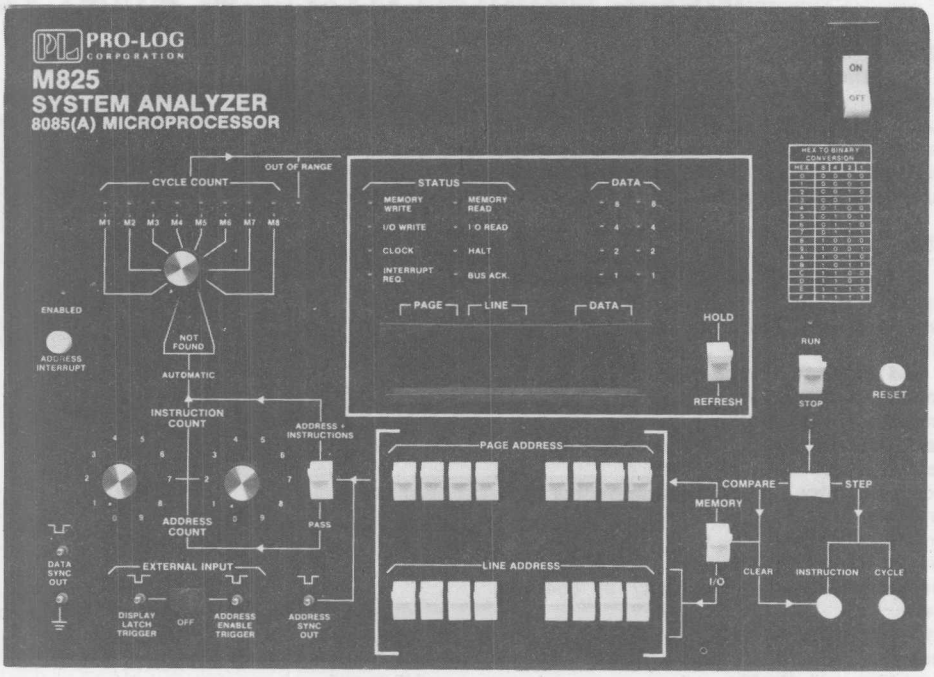
The M825 is self-contained and easily connected to your system microprocessor by means of a single DIP clip or low-profile connector. It is useful as an alternative or complement to software techniques for program development or debugging of 8085-based microprocessor systems. Since it is easily attached, the M825 system analyzer, together with adequate program documentation, is an ideal tool for field service or production.

The analyzer allows examination of the system (address, data, and status) during a user-specified machine cycle at the desired compare address. Observation of the system is possible at full system speed or by single step-by-step instruction or machine cycle. The possible display modes are dynamic mode, in which the processor continues to run without analyzer interference, and static mode, in which the analyzer controls the processor WAIT line.

Delayed data capture affords the capability of observing a particular machine cycle up to 99 instructions past a chosen reference address. The feature also allows observing the reference address after a user-defined number of passes over that address. A two-decade address counter, coupled with a single machine cycle counter, provides the operator with the capability of simply "dialing" his way through the program under investigation. This delay capability may be extended to any number by utilizing stop/compare mode.

The M825 provides memory or I/O address selection and interrupt trap and/or stop on interrupt, along with hexadecimal address, hexadecimal binary data, and status displays. The analyzer also features an oscilloscope synchronization output pulse during address compare and data display latch time. DATA SYNC OUT can be utilized to trigger an oscilloscope at any selectable instruction cycle.

Operator-initiated functions include microprocessor push-button reset, latch display or latch display and stop at the next T2 state after trigger, stop on next address compare after trigger, and generation of nonmaskable interrupt at address compare time.



M825, Front Panel

ADDRESS CONTROLS

ADDRESS switches: Sixteen address (bit) select toggle switches, broken into two groups: page address (high order address—A8 through A15) and line address (low order address or I/O—A0 through A7); used to establish the trigger reference address.

RUN/STOP switch: Selects dynamic mode (microprocessor continues to run) or static mode (microprocessor is stopped at data latch time and may be stepped through the program).

COMPARE/STEP switch: Is only functional in stop mode and selects stop on address compare and single step on cycle or instruction.

MEMORY I/O switch: Selects examination of data flow to/from memory location defined by page and line address switches, or I/O device defined by the low-order (line) address switches.

HOLD/REFRESH switch: Controls latching of the data display. In HOLD, the display is frozen the first time the selected compare condition is met. In REFRESH, the display is refreshed each time the selected compare condition is met.

DELAYED DATA CAPTURE CONTROLS

ADDRESS+INSTRUCTION/PASS toggle switch: Address+instruction mode allows data selection and display at an address up to 99 instructions beyond compare address. Pass mode allows up to 99 passes through a selected address before data is displayed.

ADDRESS COUNT/INSTRUCTION COUNT rotary switch: Controls the number of address passes in pass mode, the number of additional instructions in address+instruction mode.

CYCLE COUNT rotary switch: Selects machine cycle of interest.

ADDRESS INTERRUPT PUSH-BUTTON

ADDRESS INTERRUPT: Activation of this push-button will set an address compare latch and the next occurrence of address compare will generate a nonmaskable interrupt. Appropriate interrupt service routines must be supplied by the user and located at the required memory location. If the analyzer is stopped by address compare, the interrupt will be generated at the next address compare time.

DISPLAYS

ADDRESS: Displays 16-bit address as 4 hexadecimal digits within a range of 0000-FFFF.

DATA: A 2-digit hexadecimal display and two groups of eight bit indicators, providing binary and hexadecimal data representation.

STATUS: Eight individual indicators showing data and machine status.

MEMORY READ/WRITE and I/O READ/WRITE: Indicate the function associated with the data being displayed.

CLOCK: Indicates the processor clock is operational.

INTERRUPT REQ: Indicates a system interrupt has occurred.

HALT: Indicates the processor is in the halt state.

BUS ACK: Indicates the processor has acknowledged and responded to a bus request.

RUN/STOP: Indicates status of the machine READY line; RUN for program execution, STOP for processor idle (WAIT state).

CYCLE COUNT: Machine cycle indicator showing the cycle of the instruction with which the displayed data is associated.

NOT FOUND: Indicates that the selected machine cycle was not found.

ENABLED: Indicates the address interrupt feature is enabled.

OUT-OF-RANGE: Indicates a machine cycle greater than eight is being displayed.

SYNC POINTS

ADDRESS SYNC OUT: Provides a negative pulse out for oscilloscope triggering each time the selected address compares with the system address lines.

DATA SYNC OUT: Provides a delayed negative pulse out for oscilloscope triggering each time the analyzer data display is latched. The delay is a function of the setting of address/instruction+ machine cycle count selectors.

DISPLAY LATCH TRIGGER IN: Each negative input edge causes the analyzer to latch data at the next T2 time. If the display selector is in the hold mode, address and data are latched for each negative edge and all address compare data is locked out. If the analyzer is in the stop mode, the system can thus be halted by the external event.

ADDRESS ENABLE TRIGGER IN: For each negative input edge, an address compare latch will be set and the next address compare occurring will stop the system via the WAIT line, whether or not the analyzer is in the run mode. Depressing CLEAR will release the system and reset the latch.

GROUND pin: Ground provided for all outputs and triggers.

USER SYSTEM REQUIREMENTS

The READY, RESET IN, and TRAP lines must be capable of being wire-ORed. All interrupt lines must be strapped inactive if not used. A gate isolation resistance of 100Ω to 220Ω is recommended.

MAXIMUM μP CLOCK FREQUENCY: 3.2 MHz

LOADING SPECIFICATIONS

Inputs:

Address, data, clock, and system control lines	0.125 TTL loads @ 50 pF
INTR, RST 7.5, RST 6.5, and RST 5.5	0.25 TTL loads @ 50 pF
READY, RESET IN	1.6 TTL loads @ 100 pF
TRAP	0.125 TTL loads @ 100 pF
Display latch and address enable trigger	1.6 TTL loads @ 50 pF

Outputs:

READY, RESET IN	8 TTL loads
TRAP	ON: Source 40 mA (min) to +5V OFF: Open circuit
Address and data sync out	1 TTL load

M825, 8085(A) SYSTEM ANALYZER

POWER REQUIREMENTS

50/60 Hz 115 VAC @ 0.75 A, or
50/60 Hz 230 VAC @ 0.300 A

PHYSICAL CHARACTERISTICS

Analyzer Control Unit
Height - 4.5 in. (114.3 mm)
Width - 21 in. (533.4 mm)
Length - 12 in. (304.8 mm)

Buffer Module and Cables
Height - 1.125 in. (28.58 mm)
Width - 2.5 in. (63.5 mm)
Length - 4.5 in. (114.3 mm)

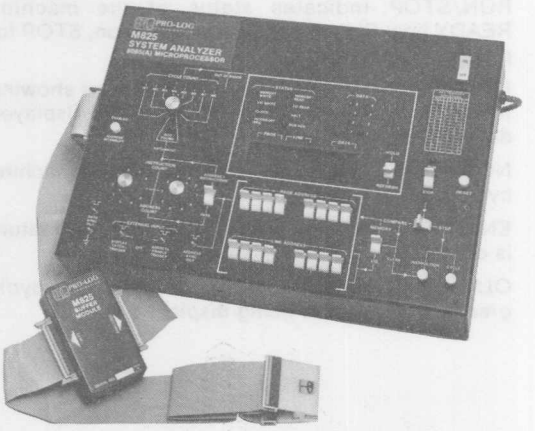
Attaché Case
Height - 6.5 in. (165.1 mm)
Width - 12.5 in. (317.5 mm)
Length - 23 in. (584.2 mm)

Total product weight is less than 15 pounds (6.80 kg).

OPERATING TEMPERATURE: 0°C to +45°C

M825 INCLUDES:

- Analyzer control unit
- Plug-in buffer module and cable
- 40-pin DIP clip connector assembly
- 40-pin low-profile connector assembly
- Attaché case
- Two copies of Ooerating manual



USER's MANUAL

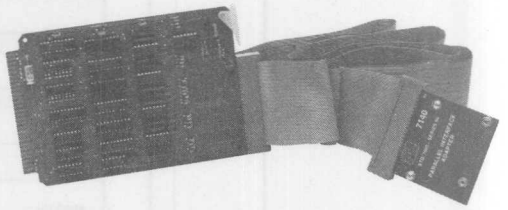
To obtain the user's manual for the M825, ask for Pro-Log document #105332.

PIN114
PARALLEL INTERFACE

PIN114 PARALLEL INTERFACE FOR STD BUS

The PIN114 supplies an 8-bit parallel interface between STD BUS systems and Pro-Log's series 90 PROM programmers equipped with parallel interface options. The PIN114 provides the hardware interface that allows a bidirectional transfer of data fields between the user's STD BUS system and the PROM programmer. Data transfer is asynchronously controlled through handshake lines.

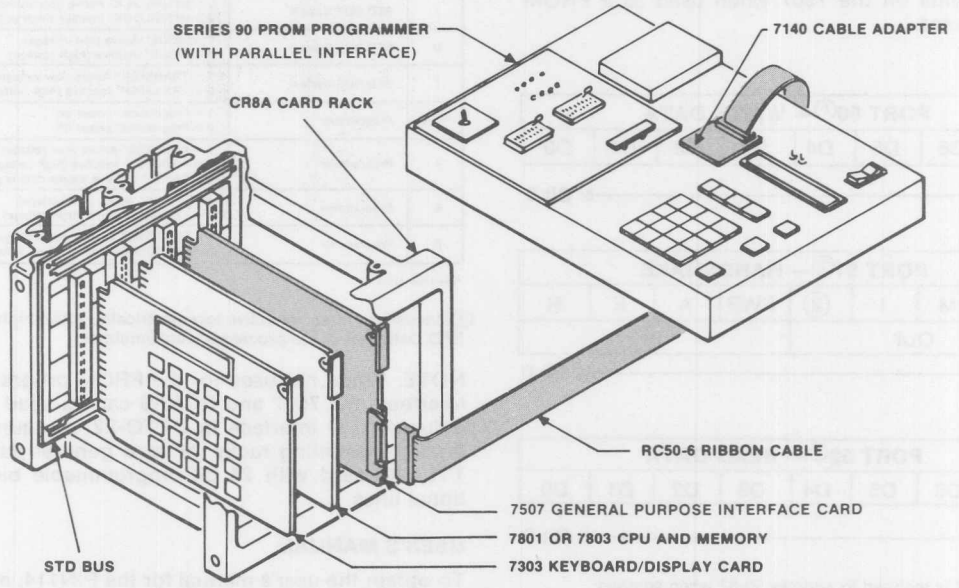
The PIN114 is immediately operational when interconnected to the STD BUS prototyping systems. Software to implement the interface is resident in the prototyping system monitor program and PROM programmer. When used with other STD BUS systems, specific software requirements and flowcharts may be found in the PROM programmer operating manuals.



FEATURES

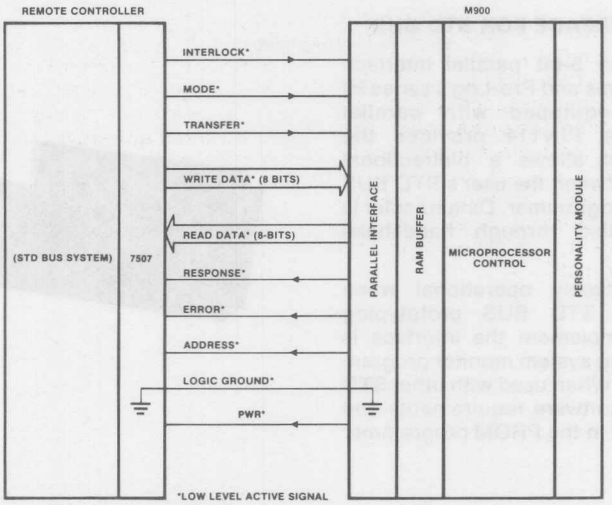
The PIN114 includes:

- **7507 general purpose interface card**
- **7140 parallel interface adapter**
- **RC50-6 ribbon cable interconnect**



System Interconnect

PIN114 PARALLEL INTERFACE OPTION



Parallel Interface — Data and Signals

The following diagrams describe the port/bit assignments on the 7507 when used as a PROM programmer.

PORT 50① — WRITE DATA							
D7	D6	D5	D4	D3	D2	D1	D0

Bit 7 ◄——► Bit 0

PORT 51① — HANDSHAKE							
T	M	I	②	PWR	A	E	R
Out				In			

Bit 7 ◄——► Bit 0

PORT 52① — READ DATA							
D7	D6	D5	D4	D3	D2	D1	D0

Bit 7 ◄——► Bit 0

① The 7507 is mapped to address 50-52 when shipped.
② Don't care.

BIT	SOURCE	LOGIC STATE [3]
I	STD BUS System	1 = INTERLOCK* Active (low voltage) 0 = INTERLOCK* Inactive (high voltage)
M	STD BUS System	1 = MODE* Active (low voltage) 0 = MODE* Inactive (high voltage)
T	STD BUS System	1 = TRANSFER* Active (low voltage) 0 = TRANSFER* Inactive (high voltage)
PWR	Programmer	1 = Programmer power on 0 = Programmer power off
A	Programmer	1 = ADDRESS* Active (low voltage) 0 = ADDRESS* Inactive (high voltage) (ADDRESS* Inactive means data is present)
E	Programmer	1 = ERROR* Active (low voltage) 0 = ERROR* Inactive (high voltage)
R	Programmer	1 = RESPONSE* Active (low voltage) 0 = RESPONSE* Inactive (high voltage)

*Low Level Active

③ Handshake lines are active low electrically, active high on the STD Data Bus or the processor's accumulator.

NOTE: When not used for the PROM programmer interface, the 7507 and RC50-6 can be used as an industrial I/O interface to OPTO-22, or equivalent module mounting racks, or as a general purpose TTL I/O card with 24 bit-programmable bidirectional lines.

USER'S MANUAL

To obtain the user's manual for the PIN114, ask for Pro-Log document #106667.

7000
STD BUS

PS1B/PS3B

STD BUS PROTOTYPING SYSTEMS

The PS1B and PS3B are two STD BUS prototyping systems designed for the 8085 and Z80 microprocessors respectively. They include: STD BUS hardware, PROM programmer and accessories, test equipment, PROM-based applications and operating software, and complete support documentation. These systems consist of the same equipment that Pro-Log uses in its Microprocessor Design Course. This equipment is all that you require to design, document, and debug programs using Pro-Log's modular methods.

FEATURES

- **STD BUS microprocessor system**
- **Eight-position card rack and motherboard**
- **+5V, ±12V power supply**
- **Buffered universal PROM programmer**
- **UV erase light**
- **Parallel interface option, links STD BUS to PROM programmer**
- **System analyzer**
- **Monitor program**
- **All required manuals and miscellaneous hardware**

PS1B/PS3B STD BUS PROTOTYPING SYSTEMS

PROTOTYPING SYSTEM CONTENTS

The PS1B and PS3B each include:

Hardware

- 7801 or 7803 microprocessor card shipped with 1K RAM and a capacity for 4K RAM and 8K EPROM
- 7605 programmable I/O card with 32 individually programmable I/O lines
- 7303 keyboard/display card
- 7904 decoded utility card contains STD BUS interface and prototyping area
- 7901 card extender
- BR08H eight slot injection-molded rack
- M281 +5V, ±12V power supply

Instrumentation and test equipment

- M980 buffered universal PROM programmer with PM9052A personality module (for 2716 EPROM)
- 9103A UV erase light
- PIN114 parallel interface consisting of the 7507 industrial I/O card, RC50-6 ribbon cable interconnect, and 7140 parallel interface adapter. This provides communication capability between the STD BUS and the PROM programmer.
- M824 or M825 system analyzer
- Two blank 2716 EPROMs, two Augat sockets, and zero insertion force socket (SZ24).

Software

- MP4 monitor program consists of a monitor, debugging, and PROM programmer interface program with subroutines that can be used independently in developing new software.

Documentation

- *Series 7000 STD BUS Technical Manual*
- *Microprocessor User's Guide*
- Program assembly forms
- Programming aid card (Z80 or 8085)
- Operating instructions and listing of monitor program
- Schematics and assembly drawings
- Data sheets
- User's manuals

Memory

- Required access time: 0.45 μs or faster
- PROM memory: 2716 or compatible
- RAM memory: 2114L

ENVIRONMENTAL SPECIFICATIONS

- Operating temperature: 0°C to 45°C at sea level

The PS1B (8085) and the PS3B (Z80) are both available in 115V and 230V configurations.

ELECRICAL SPECIFICATIONS

M281 Power Supply	
Outputs	+5V ±5% ±12V ±5%
Current	5V: 10A each +12: 1A each

Power Supply Outputs

	PS1	PS3
Executes processor instructions	8085	Z80
Time state cycle	0.320 μs	0.400 μs
Number of time states/instruction	4-18	4-23

Instruction Execution Timing

POWER REQUIREMENTS

CARD TYPE CURRENT	7801 8085 CPU	7803 Z80 CPU	7303 KEYBOARD/ DISPLAY	7605 TTL I/O	7507 I/O MODULE INTERFACE	7904 UTILITY I/O
Maximum	1400mA	1650mA	600mA	700mA	1000mA	170mA
Typical	1000mA	1150mA	300mA	450mA	750mA	90mA

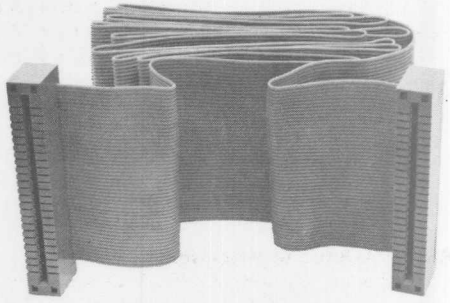
(All cards operate at +5V ±5%)

ORDERING INFORMATION			
MODEL NO.	μP	PROGRAMMER RAM BUFFER (Bytes)	INPUT VOLTAGE (VAC)
PS1B-4 (1)	8085	4K	115
PS1B-4 (2)	8085	4K	230
PS1B-8 (1)	8085	8K	115
PS1B-8 (2)	8085	8K	230
PS1B-16 (1)	8085	16K	115
PS1B-16 (2)	8085	16K	230
PS3B-4 (1)	Z80	4K	115
PS3B-4 (2)	Z80	4K	230
PS3B-8 (1)	Z80	8K	115
PS3B-8 (2)	Z80	8K	230
PS3B-16 (1)	Z80	16K	115
PS3B-16 (2)	Z80	16K	230

7000 STD BUS

RC50-6 RIBBON CABLE INTERCONNECT

The RC50-6 interfaces the 7507 I/O module mounting rack interface card to an OPTO 22 module rack for industrial control, or to the 7140 parallel interface adapter for parallel interface to the series 90 PROM programmer (PIN114).

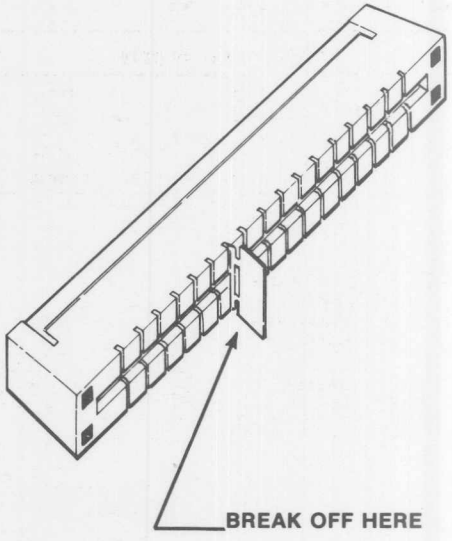


FEATURES

- **Six-foot (1.8M) long ribbon cable**
- **Contains 50 lines of #28 AWG wire**
- **Each end contains a 50-pin edge connector**
- **Includes six keys**
- **For use with 7507, 7140, and OPTO 22 module rack or equivalent**

FUNCTIONAL

Six keys are included with the RC50-6. Keys are inserted into one of the slots on the face of the connector, and the tab is then broken off. After the tab has been removed, the key should be glued into the slot if it does not fit securely.



ELECTRICAL (Typical)
(Ground-Signal-Ground Configuration)

- Impedance: 105Ω at 140kHz
- Propagation delay: 1.3 ns/ft.
- Voltage rating: 300 VRMS
- Insulation resistance: greater than $10^9\Omega$ typical

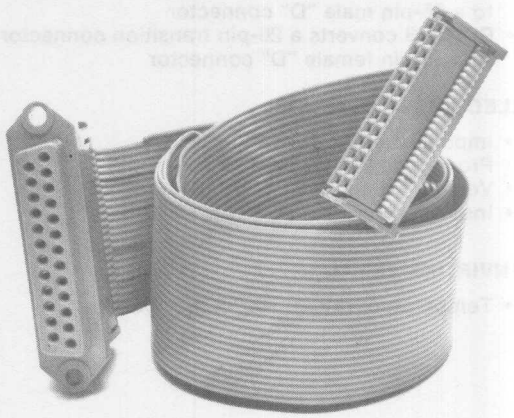
MECHANICAL

- 50 lines of #28 wire cable (7 strands of #36)
- Width: 2.45 in. (62.23 mm)
- Temperature rating: -20°C to +105°C at sea level

7000
STD BUS

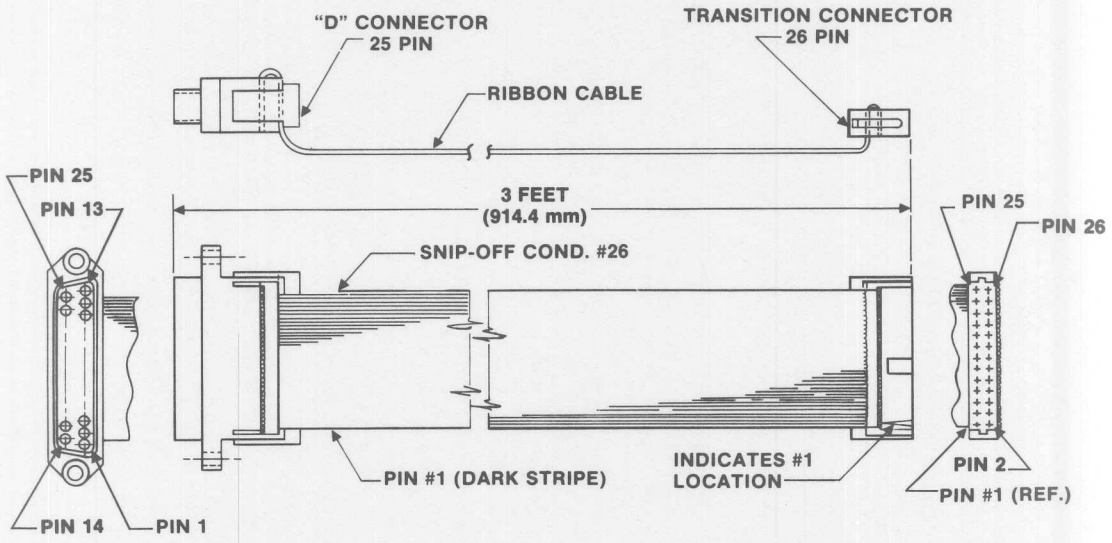
RC701-3, RC702-3 INTERCONNECT CABLE

The RC701-3 and RC702-3 are general purpose interconnect cables. Their typical application is for card to RS-232-C devices.



FEATURES

- **3-foot (914.4 mm) long ribbon cable**
- **Converts 26-pin transition connector to 25-pin "D" Connector**
- **Contains 25 lines of #28 AWG wire**



RC701-3, RC702-3 INTERCONNECT CABLE

FUNCTIONAL CAPABILITY

- RC701-3 converts a 26-pin transition connector to a 25-pin male "D" connector
- RC702-3 converts a 26-pin transition connector to a 25-pin female "D" connector

ELECTRICAL (typical)

- Impedance: 105 Ω at 140 kHz
- Propogation delay: ≤ 4.26 ns
- Voltage rating: ≥ 300V (RMS) nominal
- Insulation resistance: $> 1 \times 10^9$ Ω

ENVIRONMENTAL

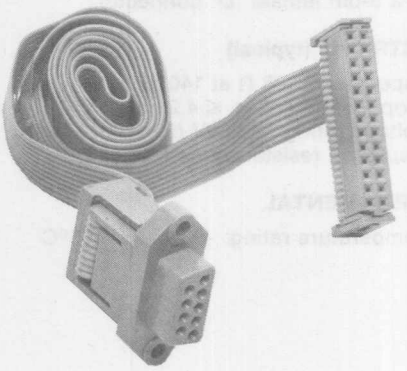
- Temperature rating: -55°C to +105°C

WIRE LIST	
"D" CONNECTOR PIN	TRANSITION CONNECTOR PIN
1	1
2	3
3	5
4	7
5	9
6	11
7	13
8	15
9	17
10	19
11	21
12	23
13	25
14	2
15	4
16	6
17	8
18	10
19	12
20	14
21	16
22	18
23	20
24	22
25	24
N/C	26

7000
STD BUS

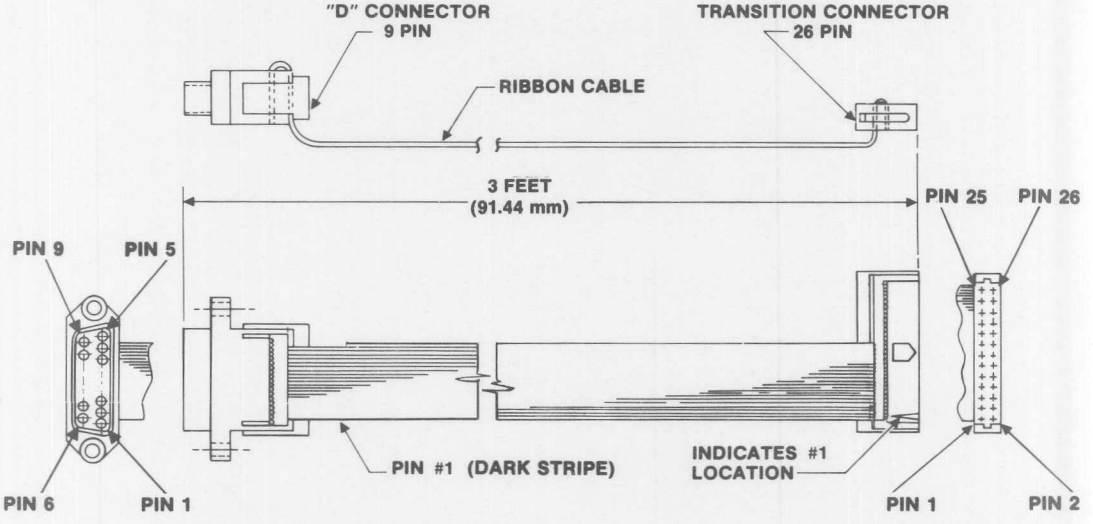
RC703-3
INTERCONNECT CABLE

The RC703-3 is a general purpose interconnect cable. Its typical application is for interconnect between the 7304 UART card and a TTY terminal.



FEATURES

- **3-foot (914.4 mm) long ribbon cable**
- **Converts 26-pin transition connector to 9-pin "D" connector**
- **Contains 9 lines of #28 AWG wire**



RC703-3 INTERCONNECT CABLE

FUNCTIONAL CAPABILITY

- RC703-3 converts a 26-pin transition connector to a 9-pin female "D" connector

ELECTRICAL (typical)

- Impedance: 105 Ω at 140 kHz
- Propogation delay: ⩽ 4.26 ns
- Voltage rating: ⩾ 300V (RMS) nominal
- Insulation resistance: > 1 X 10^9 Ω

ENVIRONMENTAL

- Temperature rating: -55°C to +105°C

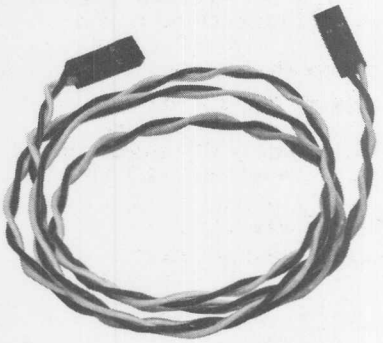
WIRE LIST	
"D" CONNECTOR PIN	TRANSITION CONNECTOR PIN
1	1
2	3
3	5
4	7
5	9
6	2
7	4
8	6
9	8
N/C	10
N/C	11
N/C	12
N/C	13
N/C	14
N/C	15
N/C	16
N/C	17
N/C	18
N/C	19
N/C	20
N/C	21
N/C	22
N/C	23
N/C	24
N/C	25
N/C	26

7000
STD BUS

RC704-1, RC704-2
INTERCONNECT CABLE

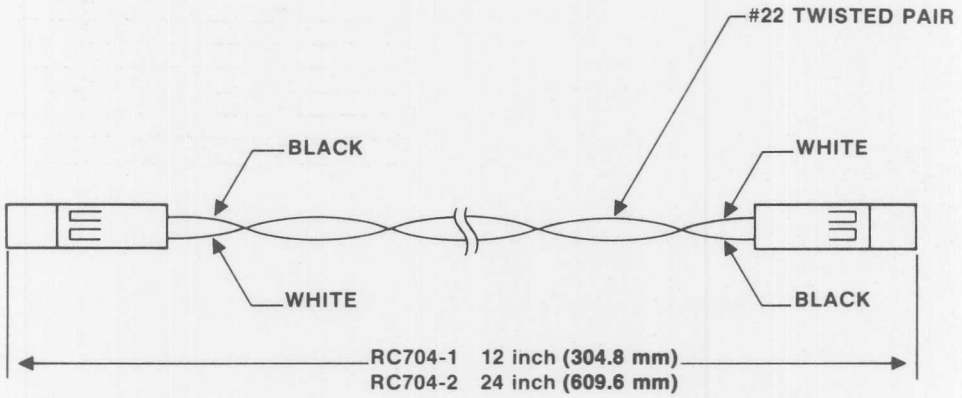
The RC704-1 and RC704-2 are general purpose interconnect cables.

Their typical application is for connecting the 7320 interrupt card to the individual interrupting devices. The cables can also connect to the 7605 I/O card for routing I/O bits to the proper locations.



FEATURES

- **Connects directly to 0.025-in. (0.64 mm) square or round post headers**
- **Each cable can handle one bit with a ground wire**
- **RC704-1 is 12 in. (304.8 mm) long**
- **RC704-2 is 24 in. (609.6 mm) long**
- **Twisted pair for noise immunity**



FUNCTIONAL CAPABILITY

This cable is used to connect single line signals to STD bus cards with 0.025-in. (0.64 mm) square or round post interface connectors on 0.1-in. centers.

ELECTRICAL (typical)

- Impedance: 105 Ω at 140 kHz
- Propogation delay: ≤ 4.26 ns
- Voltage rating: ≥ 300V (RMS) nominal
- Insulation resistance: $> 1 \times 10^9$ Ω

ENVIRONMENTAL

- Temperature rating: -55°C to +105°C

NOTES